FIG. 1

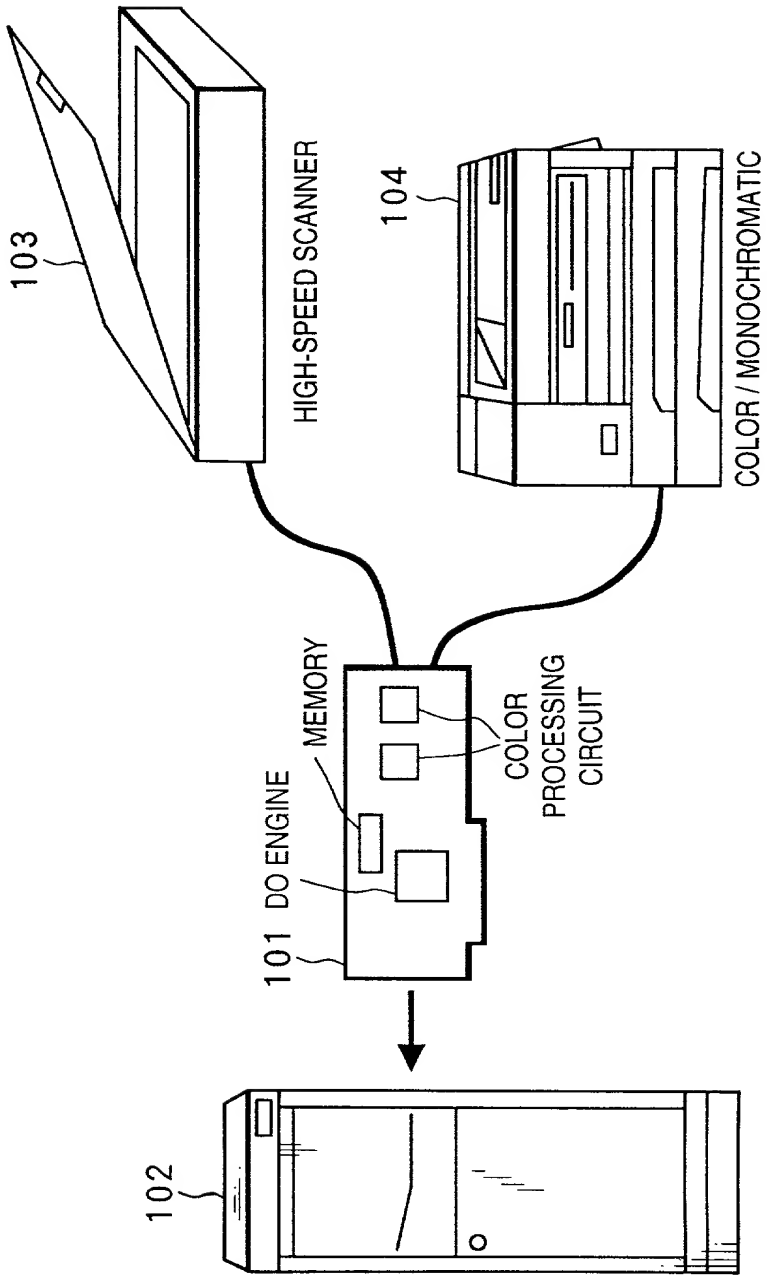

103
HIGH-SPEED SCANNER
104
COLOR / MONOCHROMATIC PRINTER
MEMORY
COLOR PROCESSING CIRCUIT
101 DO ENGINE
102

FIG. 2

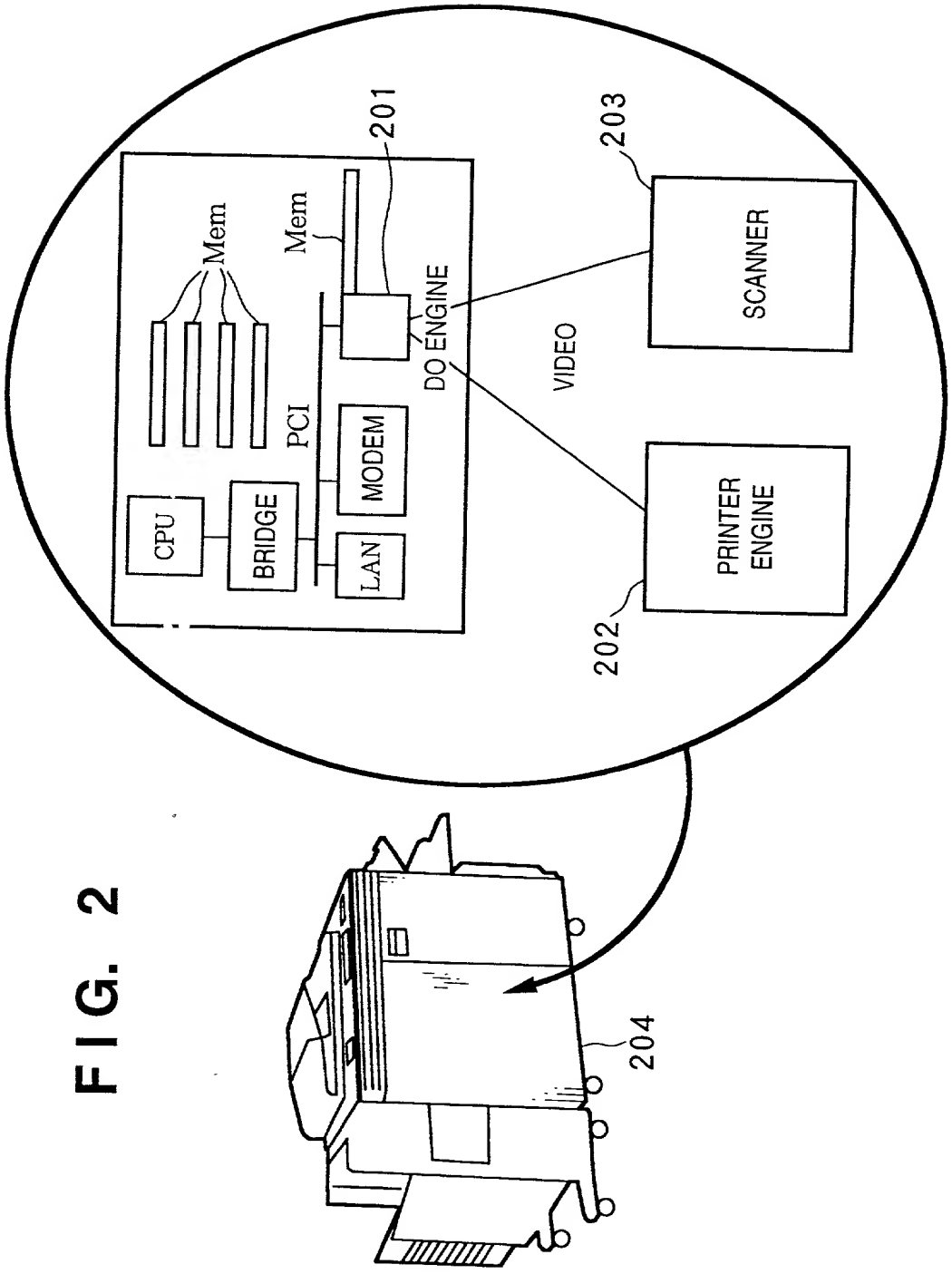

CPU
BRIDGE
Mem
Mem
PCI
MODEM
LAN
201
DO ENGINE
VIDEO
203
SCANNER
PRINTER ENGINE
202
204

FIG. 3A

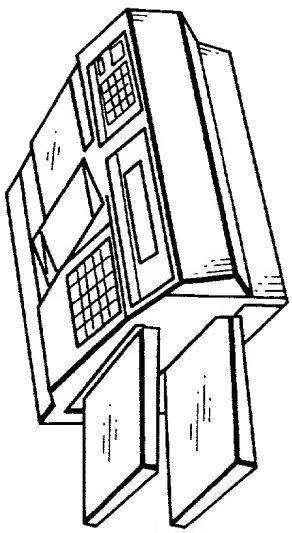


FIG. 3B

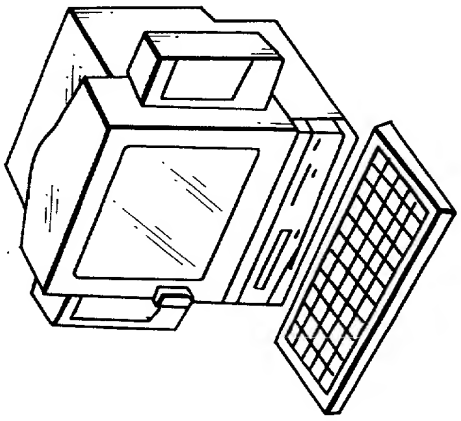
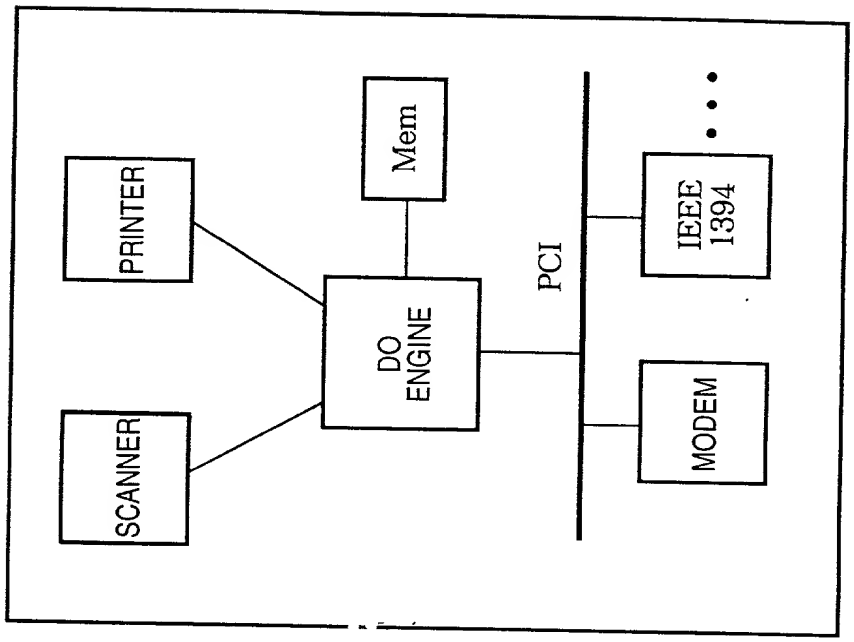


FIG. 3C



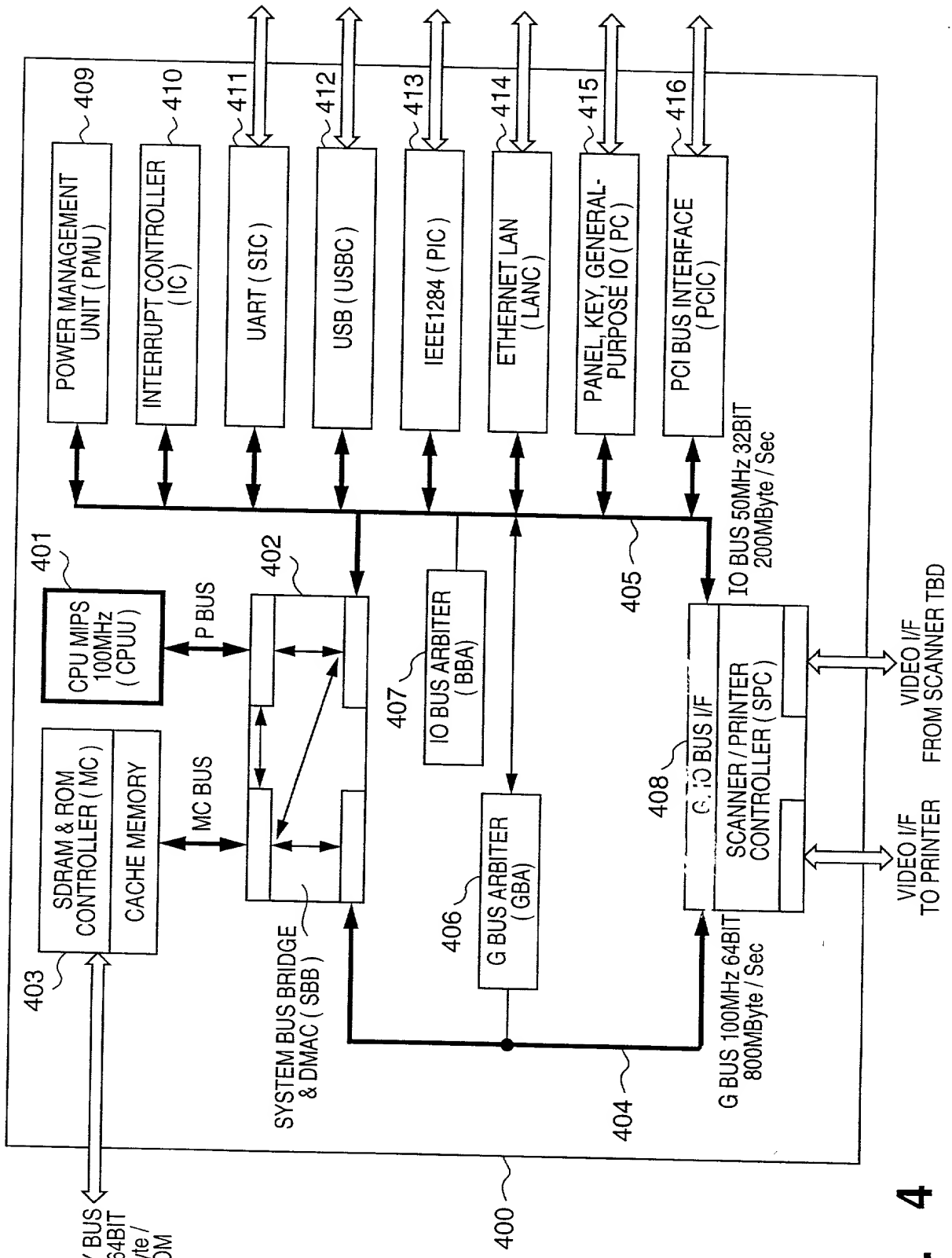

400
401
CPU MIPS 100MHz (CPUU)
P BUS
402
SYSTEM BUS BRIDGE & DMAC (SBB)
403
SDRAM & ROM CONTROLLER (MC)
CACHE MEMORY
MC BUS
MEMORY BUS 100MHz 64BIT 682MByte / Sec ROM
404
G BUS 100MHz 64BIT 800MByte / Sec
405
IO BUS 50MHz 32BIT 200MByte / Sec
406
G BUS ARBITER (GBA)
407
IO BUS ARBITER (BBA)
408
G IO BUS I/F
SCANNER / PRINTER CONTROLLER (SPC)
VIDEO I/F FROM SCANNER TBD
VIDEO I/F TO PRINTER
409
POWER MANAGEMENT UNIT (PMU)
410
INTERRUPT CONTROLLER (IC)
411
UART (SIC)
412
USB (USBC)
413
IEEE1284 (PIC)
414
ETHERNET LAN (LANC)
415
PANEL, KEY, GENERAL-PURPOSE IO (PC)
416
PCI BUS INTERFACE (PCIC)

FIG. 4

FIG. 5

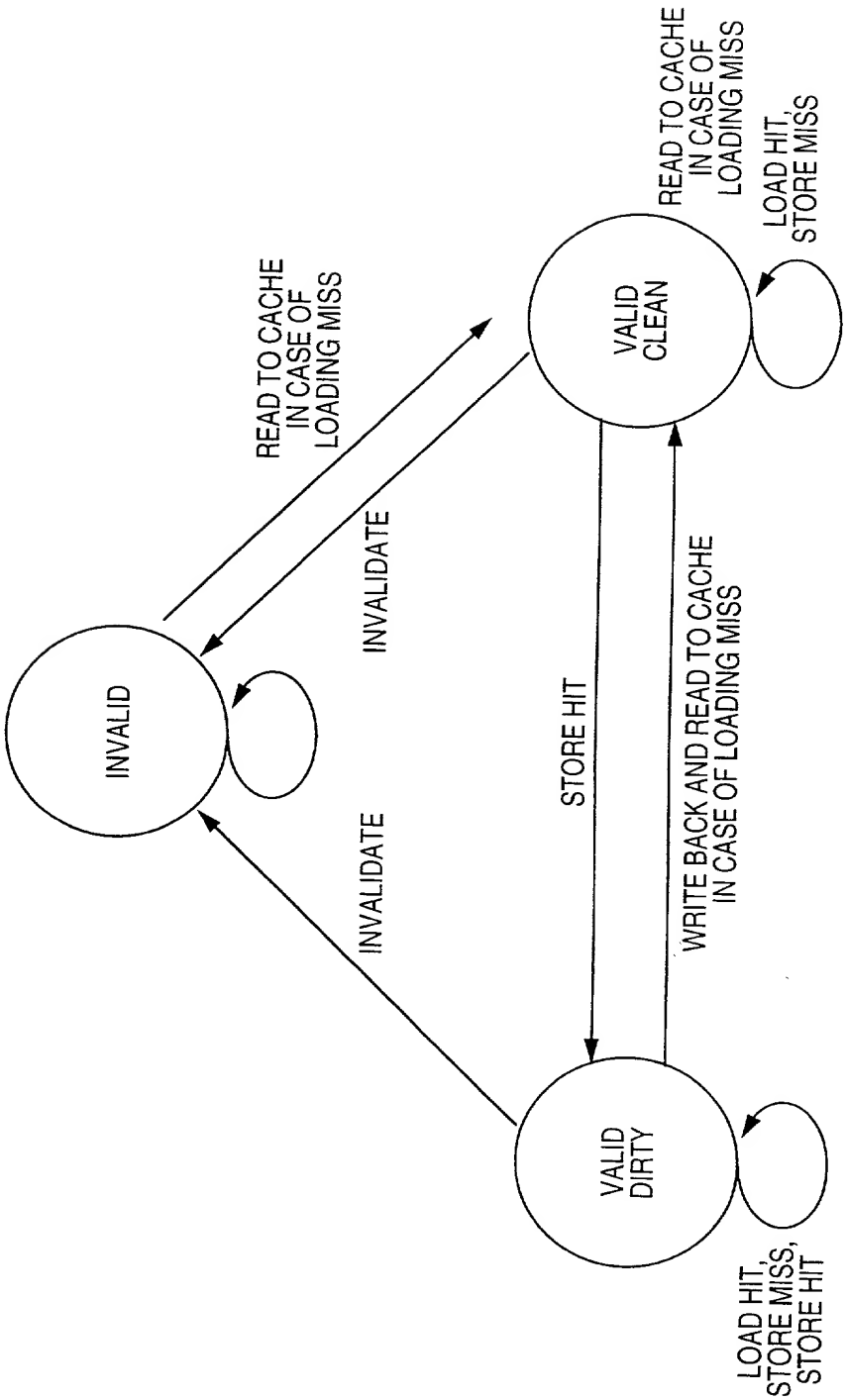

INVALID
VALID CLEAN
VALID DIRTY
READ TO CACHE IN CASE OF LOADING MISS
INVALIDATE
INVALIDATE
STORE HIT
WRITE BACK AND READ TO CACHE IN CASE OF LOADING MISS
READ TO CACHE IN CASE OF LOADING MISS
LOAD HIT, STORE MISS
LOAD HIT, STORE MISS, STORE HIT

FIG. 6

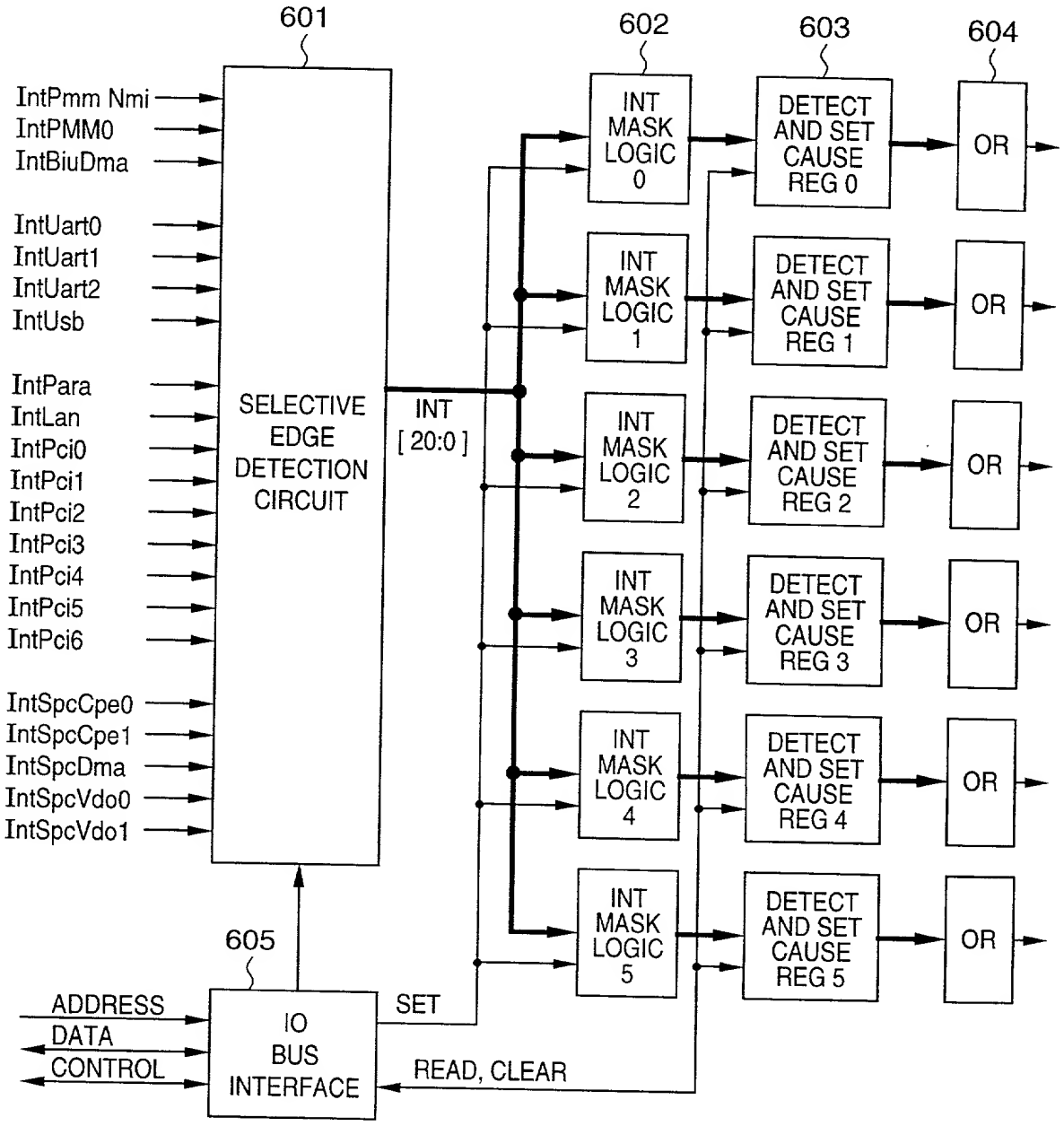

601
602
603
604
IntPmm Nmi
IntPMM0
IntBiuDma
IntUart0
IntUart1
IntUart2
IntUsb
IntPara
IntLan
IntPci0
IntPci1
IntPci2
IntPci3
IntPci4
IntPci5
IntPci6
IntSpcCpe0
IntSpcCpe1
IntSpcDma
IntSpcVdo0
IntSpcVdo1
SELECTIVE EDGE DETECTION CIRCUIT
INT [20:0]
INT MASK LOGIC 0
INT MASK LOGIC 1
INT MASK LOGIC 2
INT MASK LOGIC 3
INT MASK LOGIC 4
INT MASK LOGIC 5
DETECT AND SET CAUSE REG 0
DETECT AND SET CAUSE REG 1
DETECT AND SET CAUSE REG 2
DETECT AND SET CAUSE REG 3
DETECT AND SET CAUSE REG 4
DETECT AND SET CAUSE REG 5
OR
OR
OR
OR
OR
OR
605
ADDRESS
DATA
CONTROL
IO BUS INTERFACE
SET
READ, CLEAR

FIG. 7

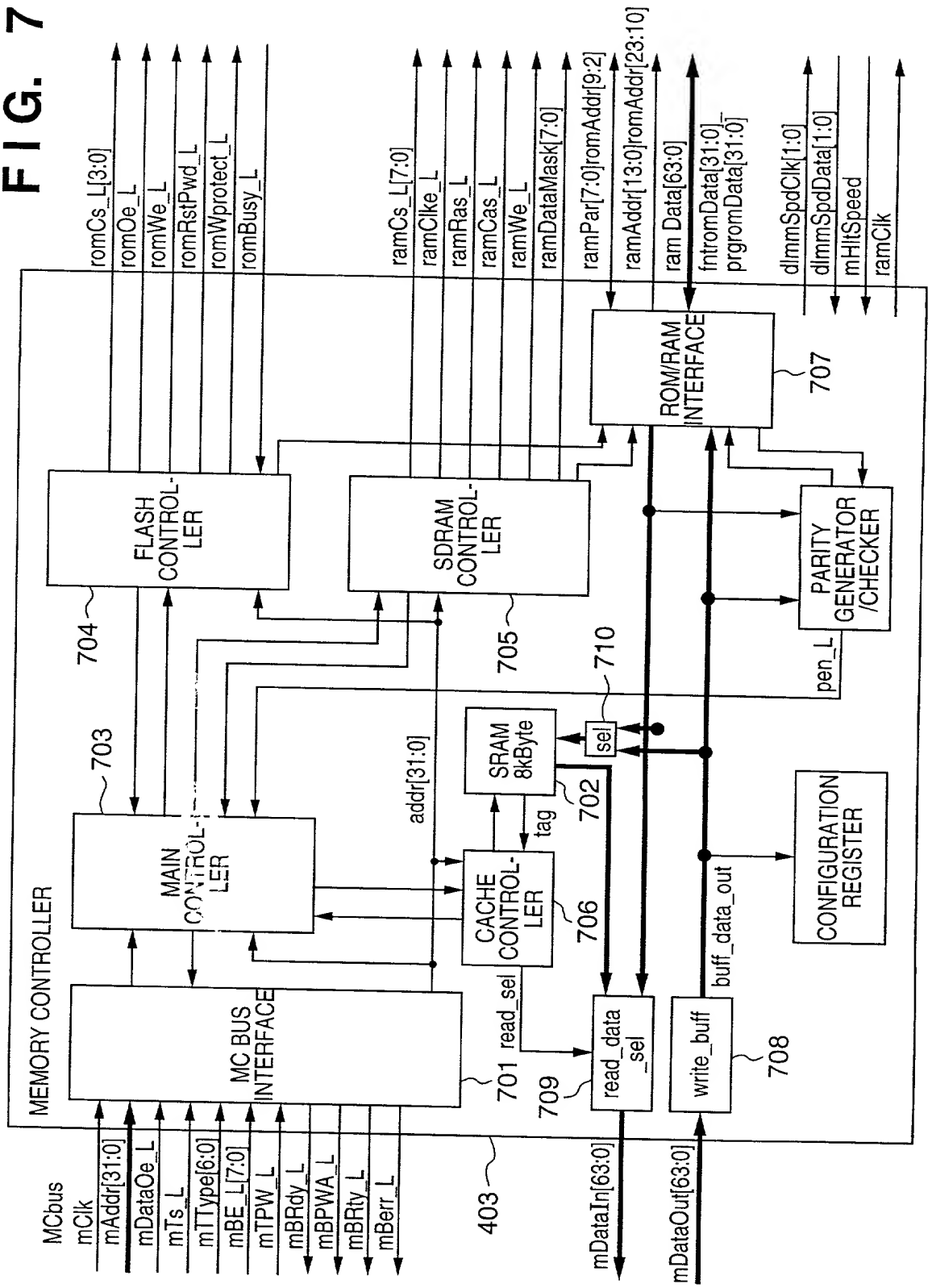

MEMORY CONTROLLER
MCbus
mClk
mAddr[31:0]
mDataOe_L
mTs_L
mTType[6:0]
mBE_L[7:0]
mTPW_L
mBRdy_L
mBPWA_L
mBRty_L
mBerr_L
403
MC BUS INTERFACE
701
MAIN CONTROL-LER
703
FLASH CONTROL-LER
704
SDRAM CONTROL-LER
705
CACHE CONTROL-LER
706
ROM/RAM INTERFACE
707
write_buff
708
read_data _sel
709
SRAM 8kByte
702
sel
710
addr[31:0]
tag
read_sel
buff_data_out
PARITY GENERATOR /CHECKER
pen_L
CONFIGURATION REGISTER
romCs_L[3:0]
romOe_L
romWe_L
romRstPwd_L
romWprotect_L
romBusy_L
ramCs_L[7:0]
ramClke_L
ramRas_L
ramCas_L
ramWe_L
ramDataMask[7:0]
ramPar[7:0]romAddr[9:2]
ramAddr[13:0]romAddr[23:10]
ram Data[63:0]
fntromData[31:0]
prgromData[31:0]
dlmmSpdClk[1:0]
dlmmSpdData[1:0]
mHltSpeed
ramClk
mDataIn[63:0]
mDataOut[63:0]

FIG. 8

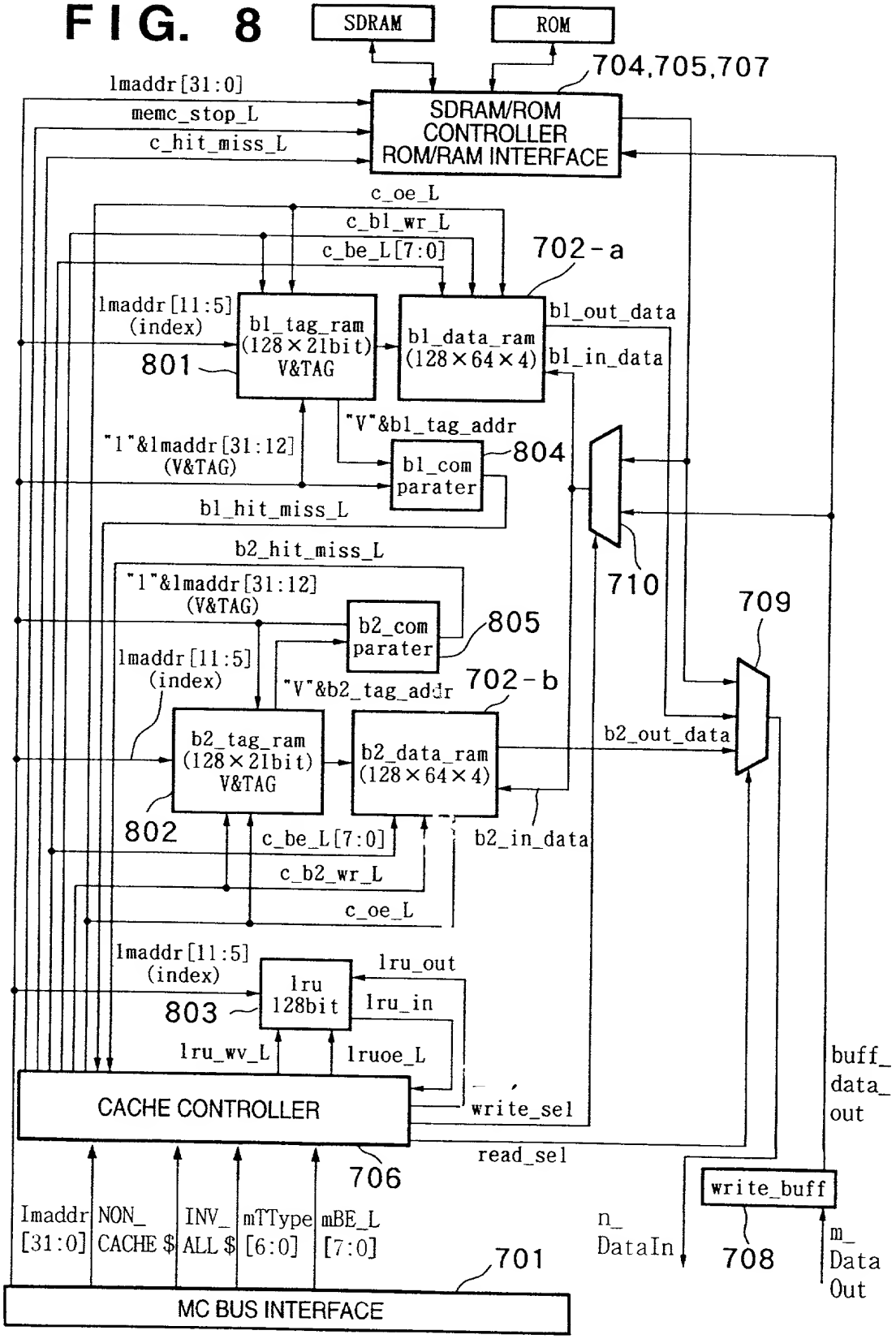

SDRAM
ROM
704,705,707
SDRAM/ROM CONTROLLER ROM/RAM INTERFACE
lmaddr[31:0]
memc_stop_L
c_hit_miss_L
c_oe_L
c_bl_wr_L
c_be_L[7:0]
702-a
lmaddr[11:5] (index)
bl_tag_ram (128×21bit) V&TAG
801
bl_data_ram (128×64×4)
bl_out_data
bl_in_data
"V"&bl_tag_addr
"1"&lmaddr[31:12] (V&TAG)
bl_com parater
804
bl_hit_miss_L
710
b2_hit_miss_L
"1"&lmaddr[31:12] (V&TAG)
b2_com parater
805
709
lmaddr[11:5] (index)
"V"&b2_tag_addr
702-b
b2_tag_ram (128×21bit) V&TAG
b2_data_ram (128×64×4)
b2_out_data
802
c_be_L[7:0]
b2_in_data
c_b2_wr_L
c_oe_L
lmaddr[11:5] (index)
lru 128bit
lru_out
lru_in
803
lru_wv_L
lruoe_L
CACHE CONTROLLER
write_sel
read_sel
706
buff_ data_ out
write_buff
n_ DataIn
708
m_ Data Out
Imaddr [31:0]
NON_ CACHE $
INV_ ALL $
mTType [6:0]
mBE_L [7:0]
701
MC BUS INTERFACE

FIG. 9

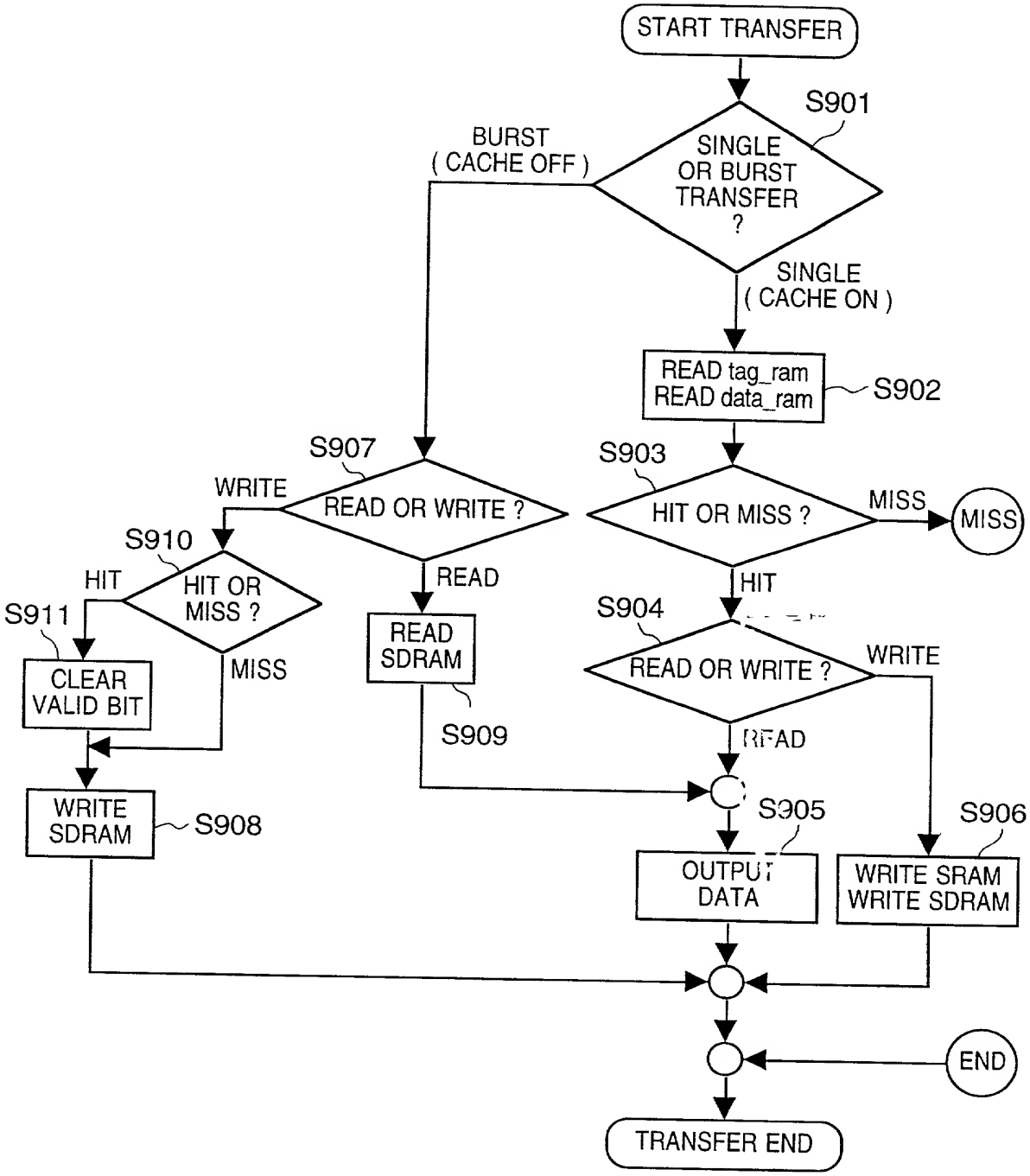

START TRANSFER
S901
SINGLE OR BURST TRANSFER ?
BURST (CACHE OFF)
SINGLE (CACHE ON)
READ tag_ram READ data_ram
S902
S903
HIT OR MISS ?
MISS
MISS
HIT
S904
READ OR WRITE ?
WRITE
READ
S907
READ OR WRITE ?
WRITE
READ
S910
HIT OR MISS ?
HIT
MISS
S911
CLEAR VALID BIT
READ SDRAM
S909
WRITE SDRAM
S908
S905
OUTPUT DATA
S906
WRITE SRAM WRITE SDRAM
END
TRANSFER END

FIG. 10

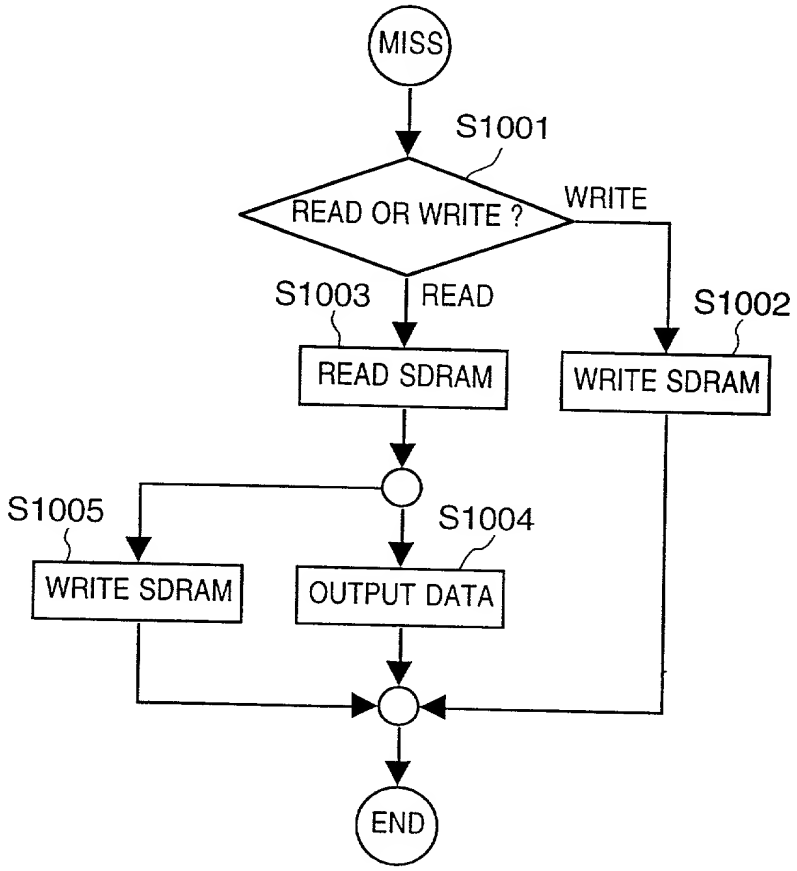

MISS
S1001
READ OR WRITE ?
WRITE
S1003
READ
S1002
READ SDRAM
WRITE SDRAM
S1005
S1004
WRITE SDRAM
OUTPUT DATA
END

FIG. 11

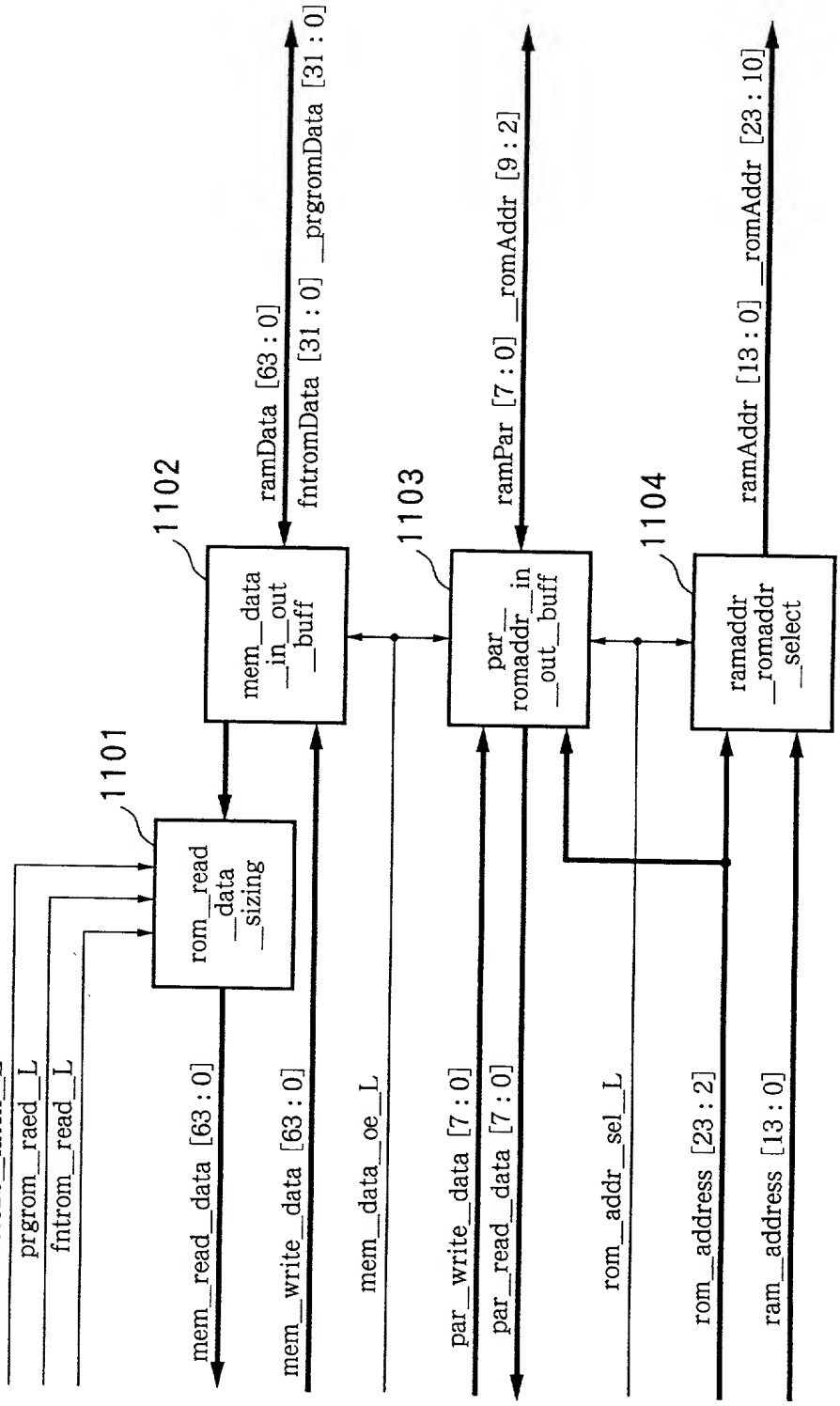

1101
1102
1103
1104
rom_read_data_sizing
mem_data_in_out_buff
par_romaddr_in_out_buff
ramaddr_romaddr_select
first32b_latch_L
prgrom_raed_L
fntrom_read_L
mem_read_data [63 : 0]
mem_write_data [63 : 0]
mem_data_oe_L
par_write_data [7 : 0]
par_read_data [7 : 0]
rom_addr_sel_L
rom_address [23 : 2]
ram_address [13 : 0]
ramData [63 : 0]
fntromData [31 : 0]
_prgromData [31 : 0]
ramPar [7 : 0]
_romAddr [9 : 2]
ramAddr [13 : 0]
_romAddr [23 : 10]

FIG. 12

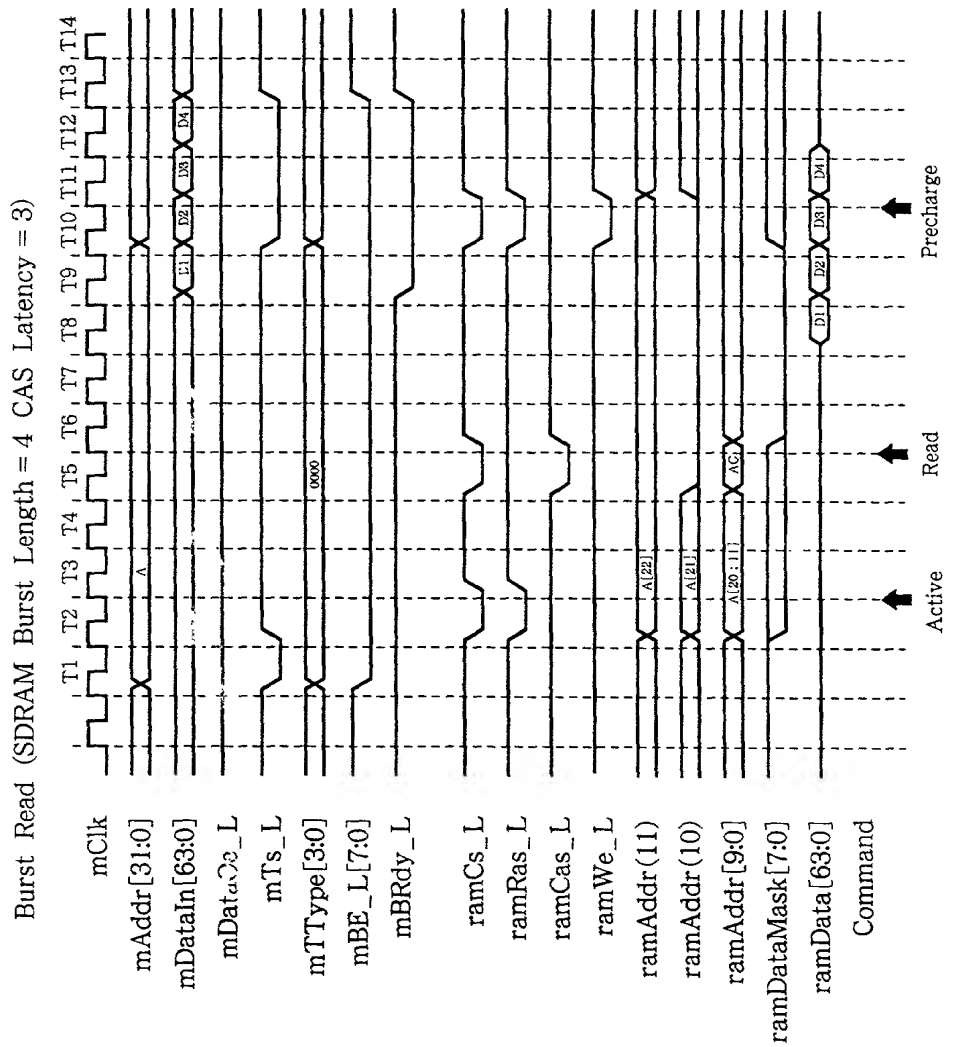
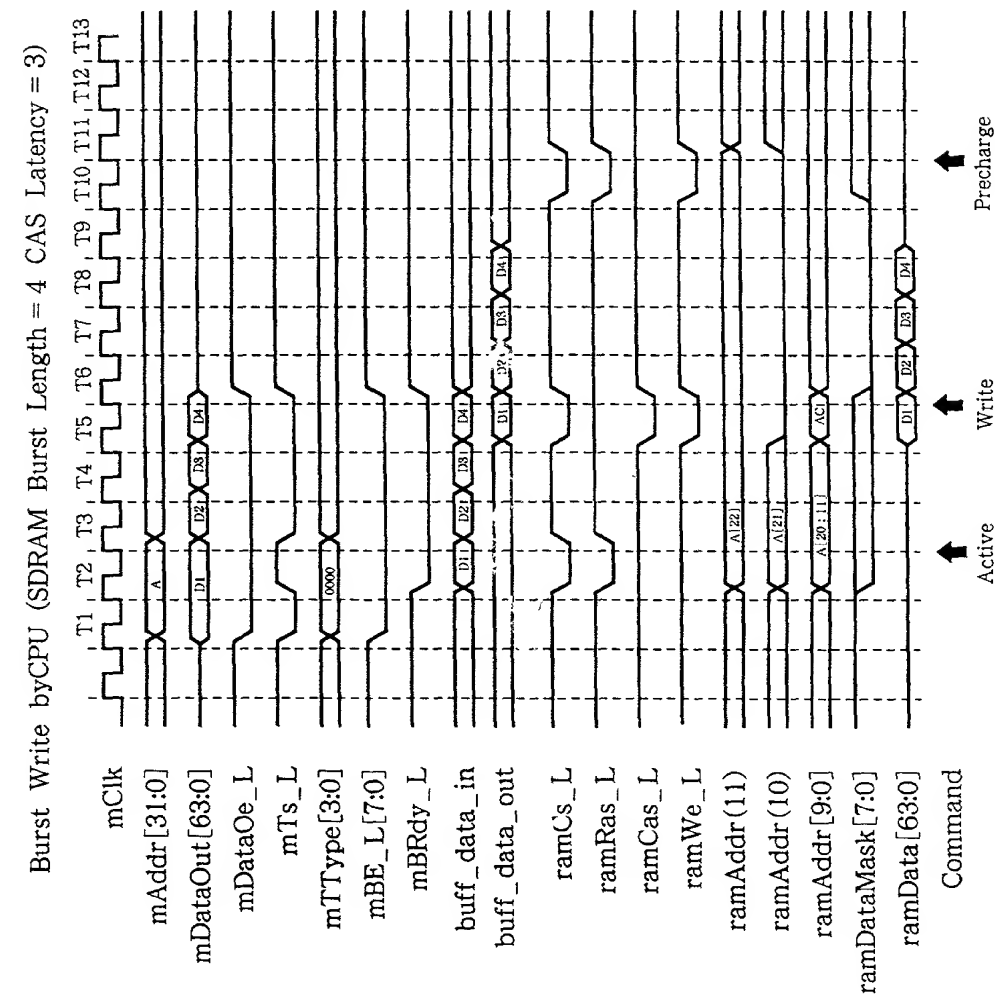

Burst Read (SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14
mClk
mAddr[31:0]
mDataIn[63:0]
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
MC BUS
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
MEMORY BUS
A
0000
A[22]
A[21]
A[20:11]
AC
D1
D2
D3
D4
Active
Read
Precharge

FIG. 13


Burst Write byCPU (SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
mClk
mAddr[31:0]
mDataOut[63:0]
mDataOe_L
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
buff_data_in
buff_data_out
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
MC BUS
MEMORY BUS
Active
Write
Precharge

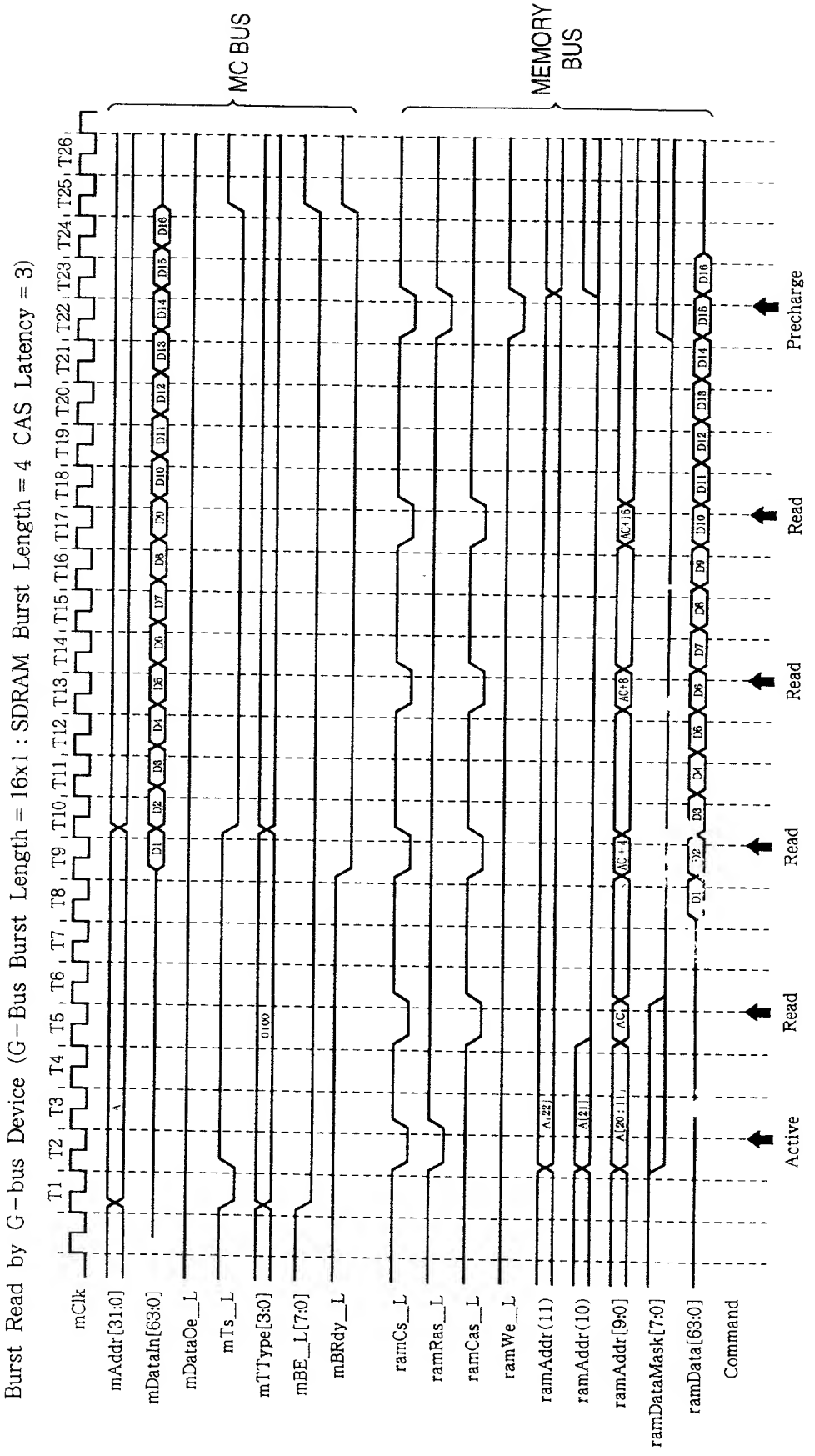

Burst Read by G-bus Device (G-Bus Burst Length = 16x1 : SDRAM Burst Length = 4 CAS Latency = 3)
MC BUS
MEMORY BUS
mClk
mAddr[31:0]
mDataIn[63:0]
mDataOe_L
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
Active
Read
Read
Read
Read
Precharge

FIG. 14

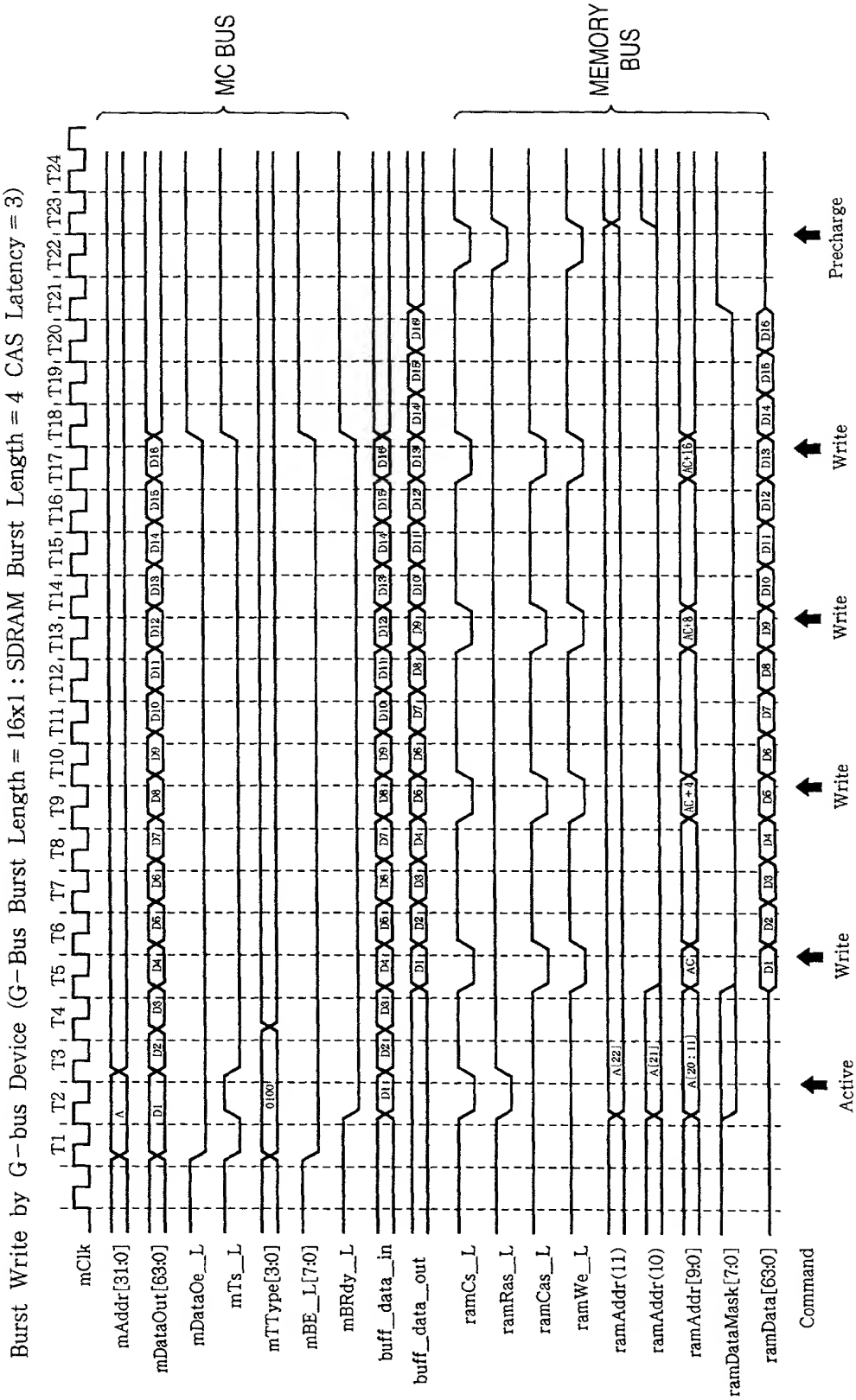

Burst Write by G-bus Device (G-Bus Burst Length = 16x1 : SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22 T23 T24
MC BUS
MEMORY BUS
mClk
mAddr[31:0]
mDataOut[63:0]
mDataOe_L
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
buff_data_in
buff_data_out
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
Active
Write
Write
Write
Write
Precharge

FIG. 15

Single Read Cache Hit (SDRAM Burst Length = 4 CAS Latency = 3)

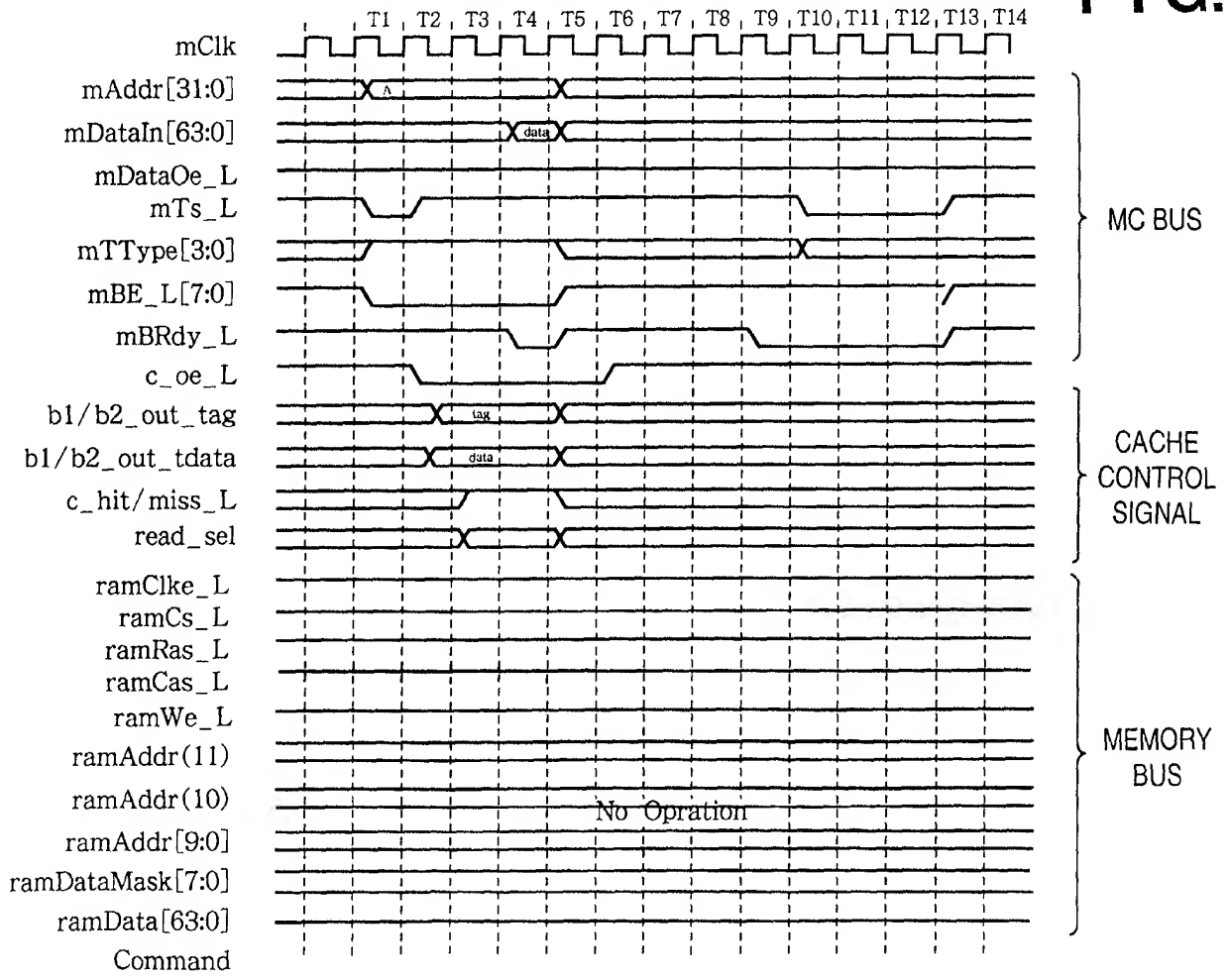
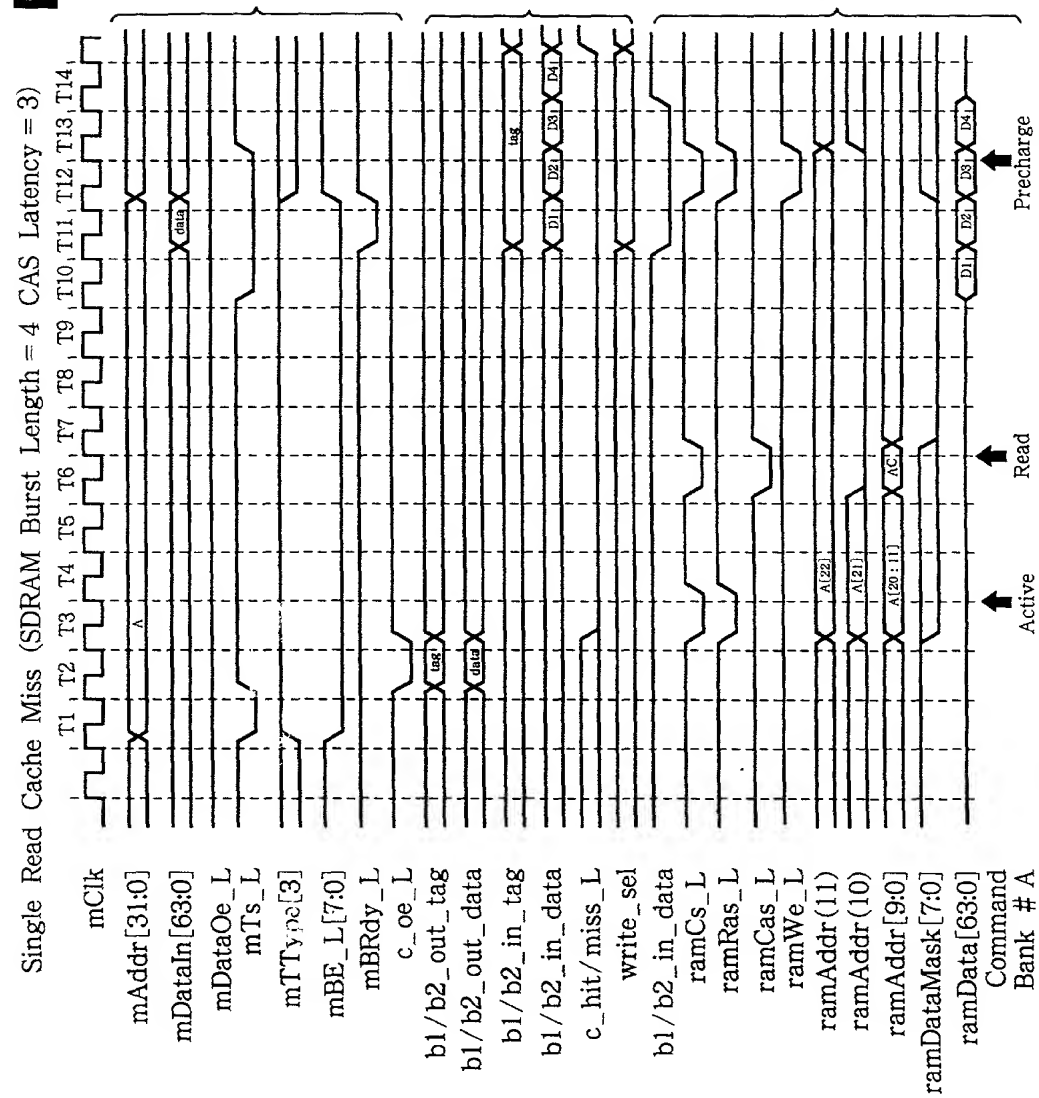


FIG. 16

FIG. 17


Single Read Cache Miss (SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14
mClk
mAddr[31:0]
mDataIn[63:0]
mDataOe_L
mTs_L
mTType[3]
mBE_L[7:0]
mBRdy_L
c_oe_L
b1/b2_out_tag
b1/b2_out_data
b1/b2_in_tag
b1/b2_in_data
c_hit/miss_L
write_sel
b1/b2_in_data
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
Bank # A
MC BUS
CACHE CONTROL SIGNAL
MEMORY BUS
A
data
tag
data
tag
D1
D2
D3
D4
A[22]
A[21]
A[20:11]
AC
D1
D2
D3
D4
Active
Read
Precharge

Single Write Cache Hit (SDRAM Burst Length = 4 CAS Latency = 3)

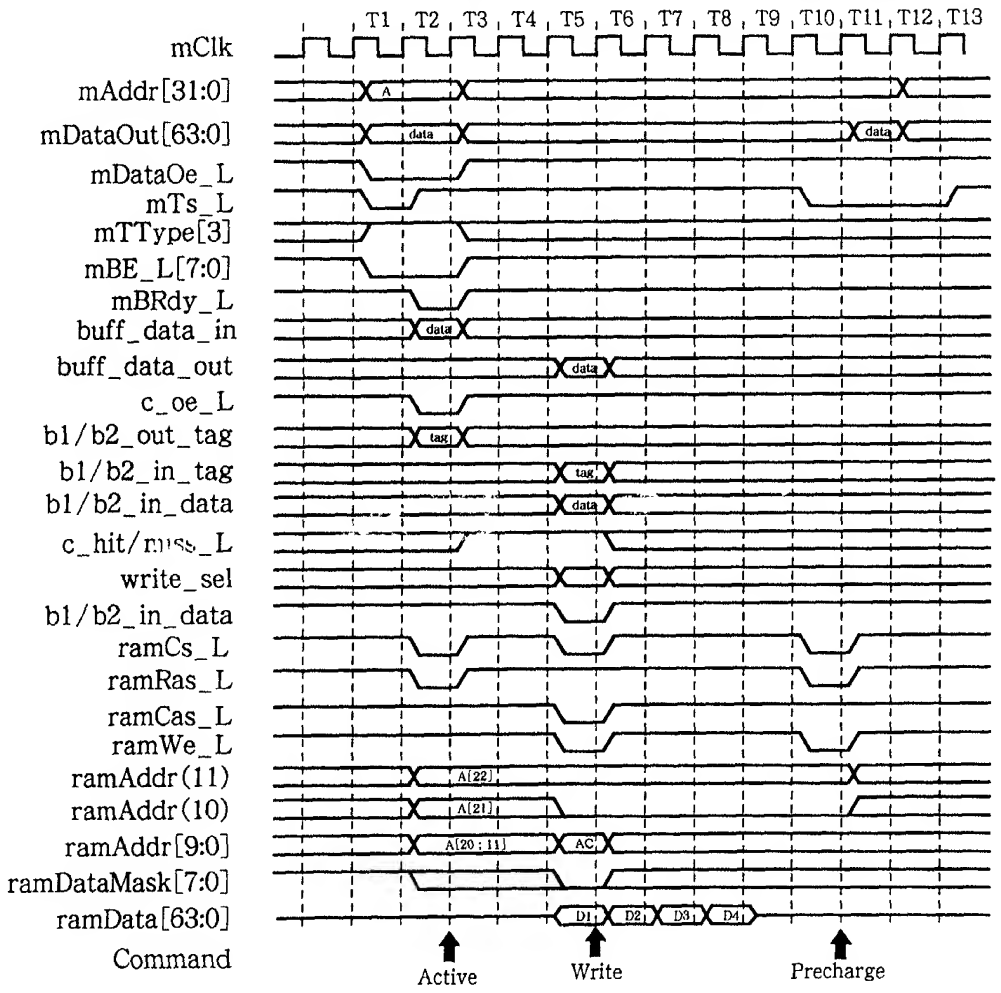
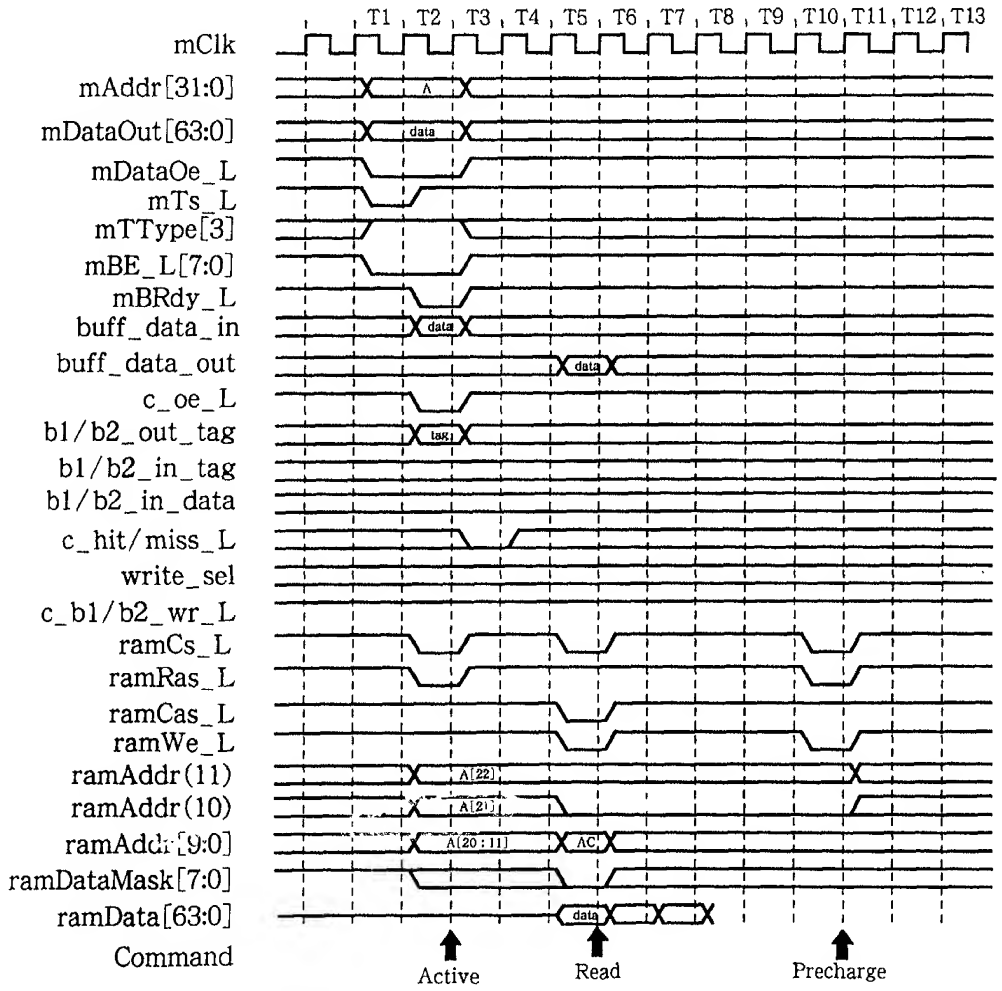


FIG. 18

Single Write Cache Miss (SDRAM Burst Length = 4 CAS Latency = 3)



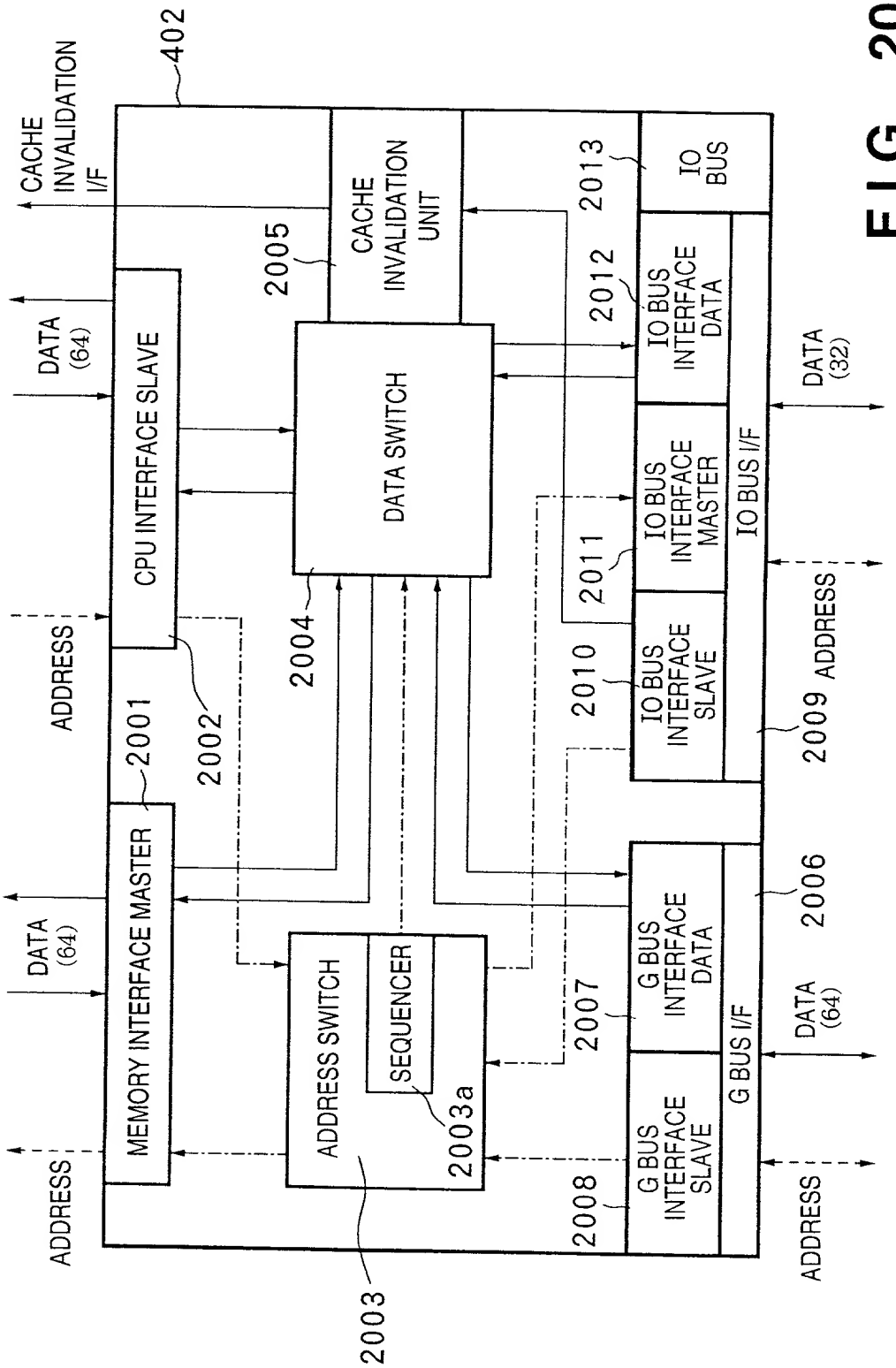

402
CACHE INVALIDATION I/F
CACHE INVALIDATION UNIT
2005
2013
IO BUS
2012
IO BUS INTERFACE DATA
DATA (64)
DATA SWITCH
DATA (32)
CPU INTERFACE SLAVE
2001
2002
2004
2011
IO BUS INTERFACE MASTER
IO BUS I/F
ADDRESS
2010
IO BUS INTERFACE SLAVE
2009
ADDRESS
MEMORY INTERFACE MASTER
DATA (64)
ADDRESS SWITCH
SEQUENCER
2003a
2007
G BUS INTERFACE DATA
2006
G BUS I/F
DATA (64)
2008
G BUS INTERFACE SLAVE
ADDRESS
ADDRESS
2003

FIG. 20

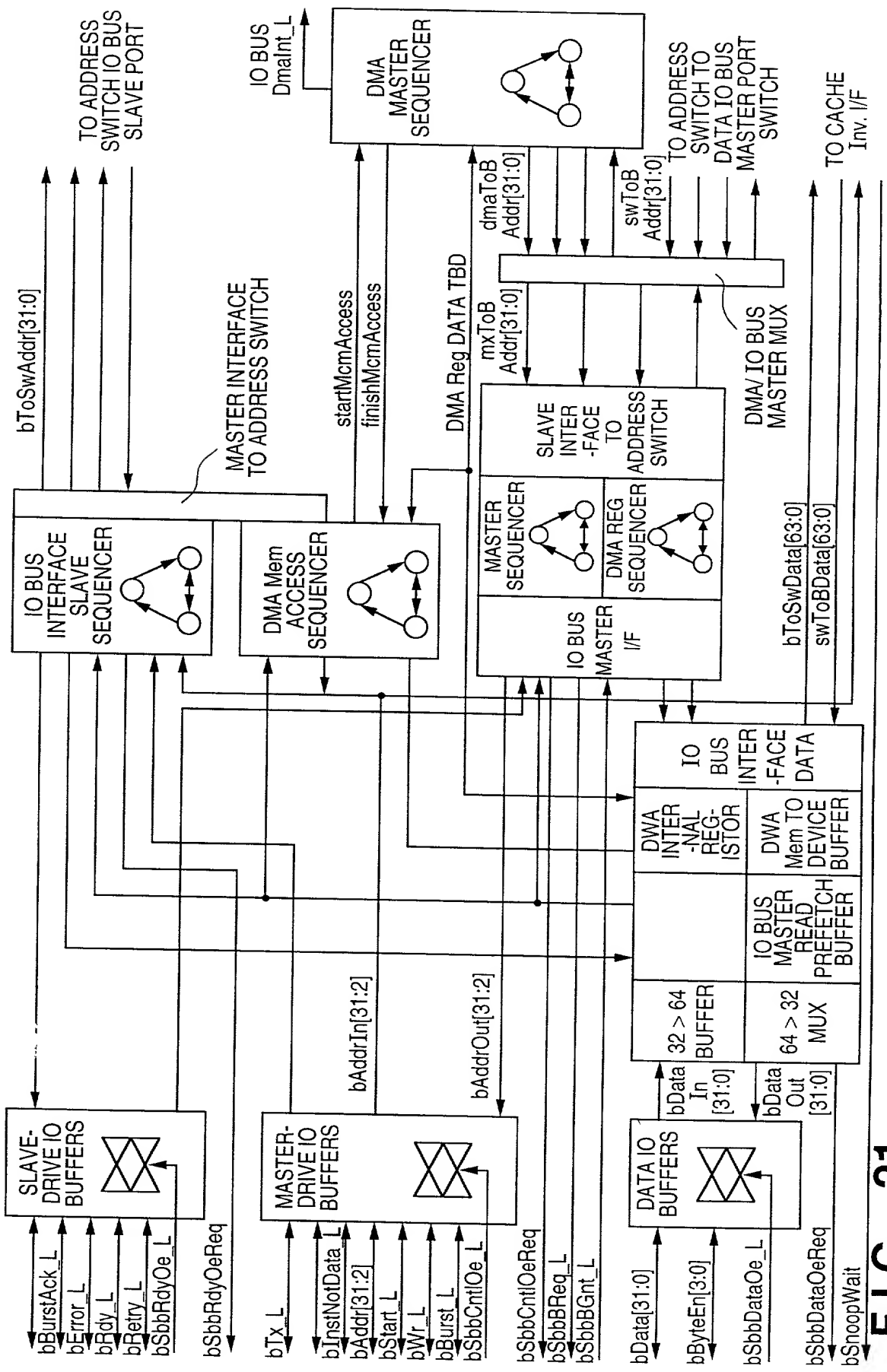

TO ADDRESS SWITCH IO BUS SLAVE PORT
IO BUS DmaInt_L
DMA MASTER SEQUENCER
TO ADDRESS SWITCH TO DATA IO BUS MASTER PORT SWITCH
TO CACHE Inv. I/F
bToSwAddr[31:0]
MASTER INTERFACE TO ADDRESS SWITCH
startMcmAccess
finishMcmAccess
DMA Reg DATA TBD
dmaToB Addr[31:0]
swToB Addr[31:0]
mxToB Addr[31:0]
SLAVE INTER -FACE TO ADDRESS SWITCH
DMA/ IO BUS MASTER MUX
IO BUS INTERFACE SLAVE SEQUENCER
DMA Mem ACCESS SEQUENCER
MASTER SEQUENCER
DMA REG SEQUENCER
IO BUS MASTER I/F
bToSwData[63:0]
swToBData[63:0]
IO BUS INTER -FACE DATA
DWA INTER -NAL REG- ISTOR
DWA Mem TO DEVICE BUFFER
IO BUS MASTER READ PREFETCH BUFFER
32 > 64 BUFFER
64 > 32 MUX
SLAVE- DRIVE IO BUFFERS
MASTER- DRIVE IO BUFFERS
DATA IO BUFFERS
bAddrIn[31:2]
bAddrOut[31:2]
bData In [31:0]
bData Out [31:0]
bBurstAck_L
bError_L
bRdy_L
bRetry_L
bSbbRdyOe_L
bSbbRdyOeReq
bTx_L
bInstNotData_L
bAddr[31:2]
bStart_L
bWr_L
bBurst_L
bSbbCntlOe_L
bSbbCntlOeReq
bSbbBReq_L
bSbbBGnt_L
bData[31:0]
bByteEn[3:0]
bSbbDataOe_L
bSbbDataOeReq
bSnoopWait

FIG. 21

FIG. 22

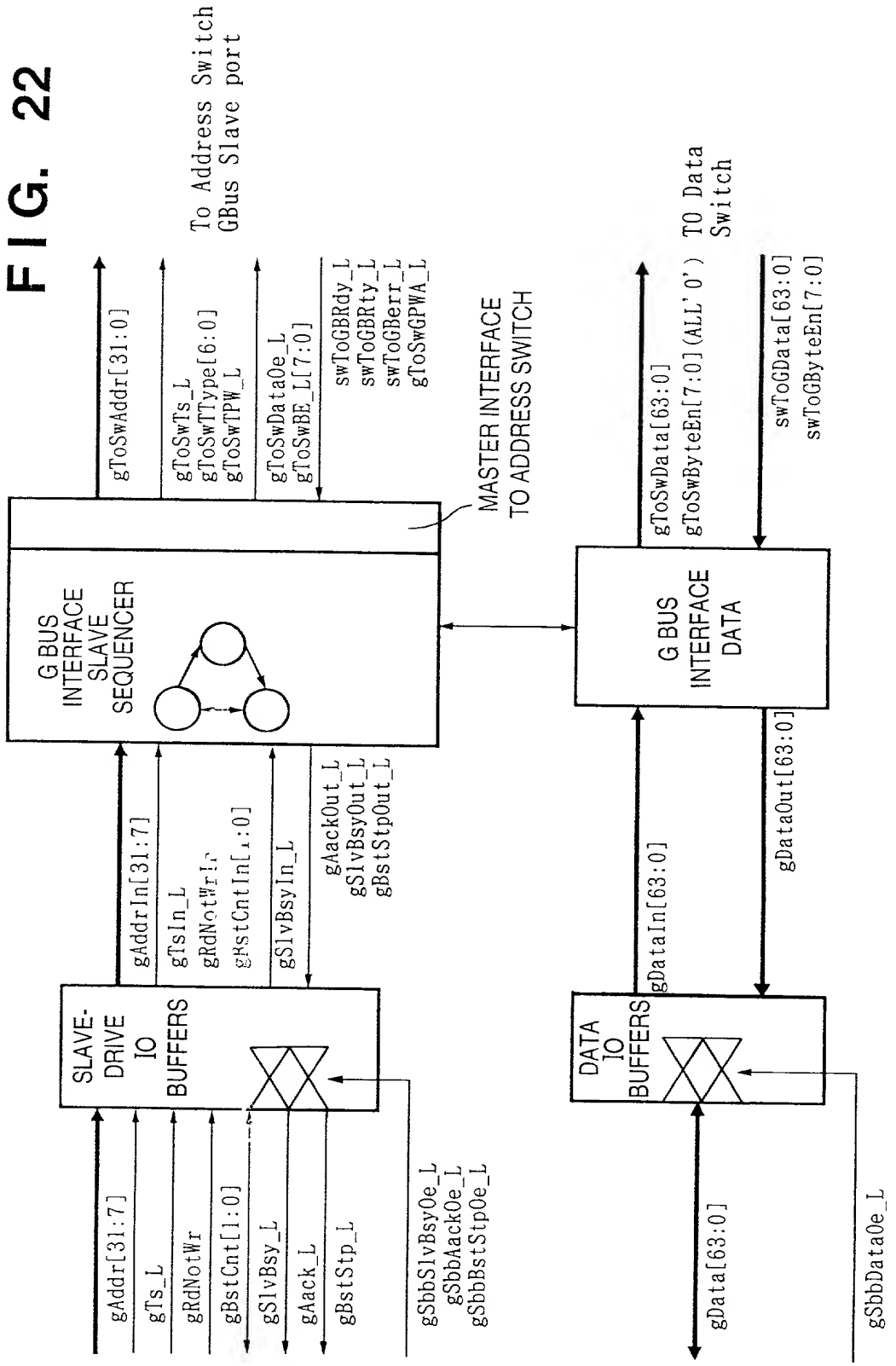

To Address Switch
GBus Slave port
gToSwAddr[31:0]
gToSwTs_L
gToSwTType[6:0]
gToSwTPW_L
gToSwDataOe_L
gToSwBE_L[7:0]
swToGBRdy_L
swToGBRty_L
swToGBerr_L
gToSwGPWA_L
MASTER INTERFACE
TO ADDRESS SWITCH
G BUS
INTERFACE
SLAVE
SEQUENCER
gAddrIn[31:7]
gTsIn_L
gRdNotWrIn
gBstCntIn[1:0]
gSlvBsyIn_L
gAackOut_L
gSlvBsyOut_L
gBstStpOut_L
SLAVE-
DRIVE
IO
BUFFERS
gAddr[31:7]
gTs_L
gRdNotWr
gBstCnt[1:0]
gSlvBsy_L
gAack_L
gBstStp_L
gSbbSlvBsyOe_L
gSbbAackOe_L
gSbbBstStpOe_L
gToSwData[63:0]
gToSwByteEn[7:0](ALL'0')
TO Data
Switch
swToGData[63:0]
swToGByteEn[7:0]
G BUS
INTERFACE
DATA
gDataIn[63:0]
gDataOut[63:0]
DATA
IO
BUFFERS
gData[63:0]
gSbbDataOe_L

FIG. 23A FIG. 23B FIG. 23C FIG. 23D

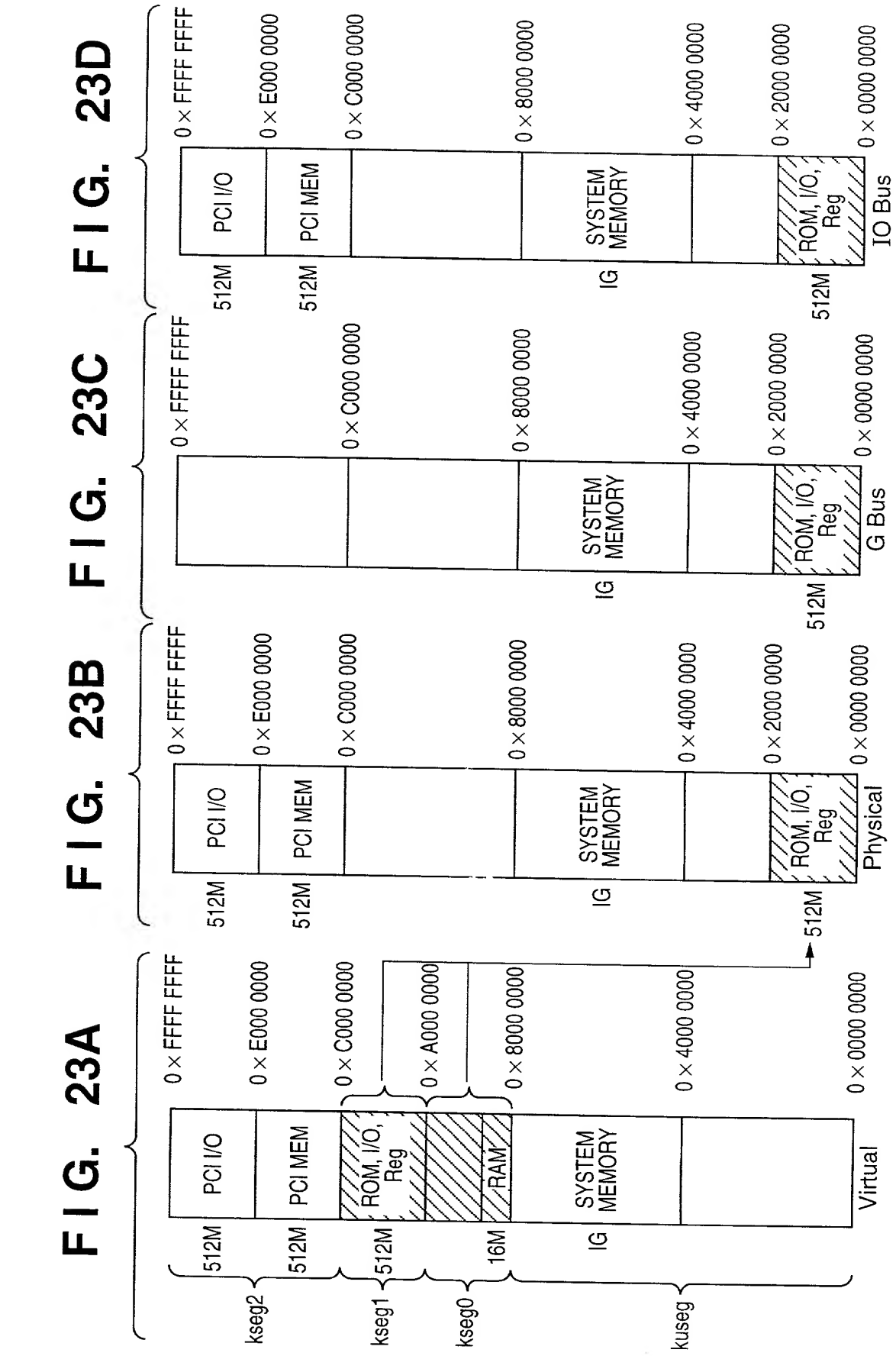


FIG. 24A

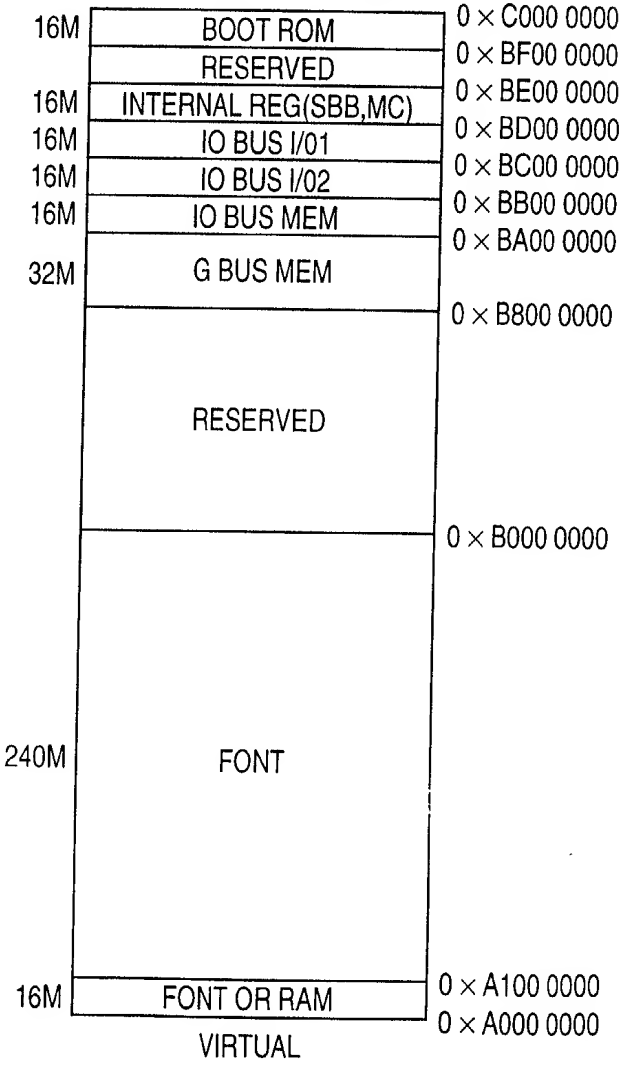


FIG. 24B

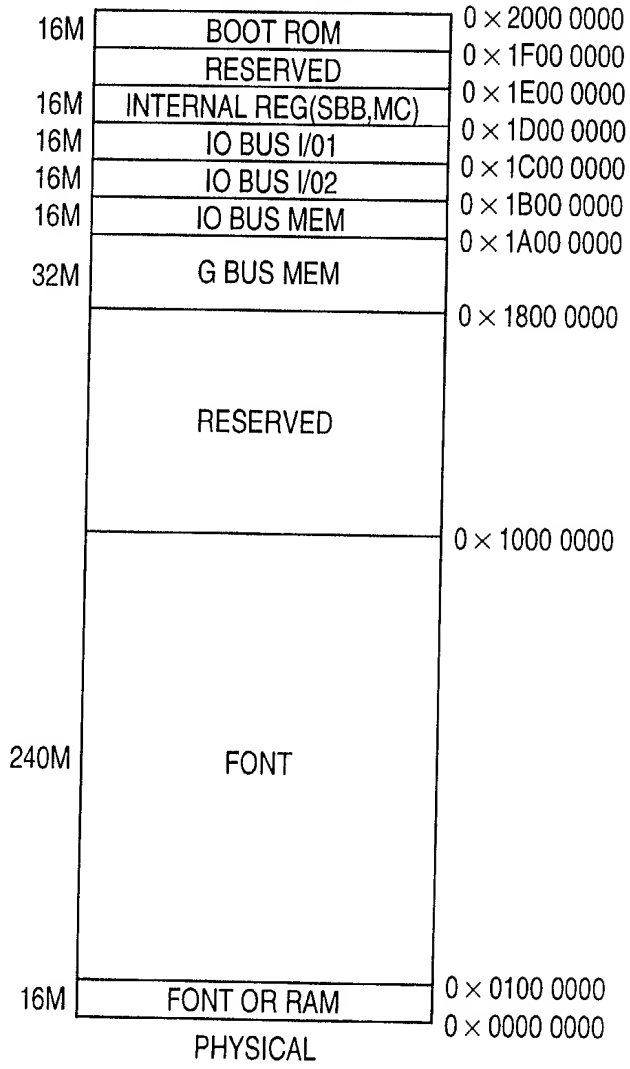


FIG. 24C

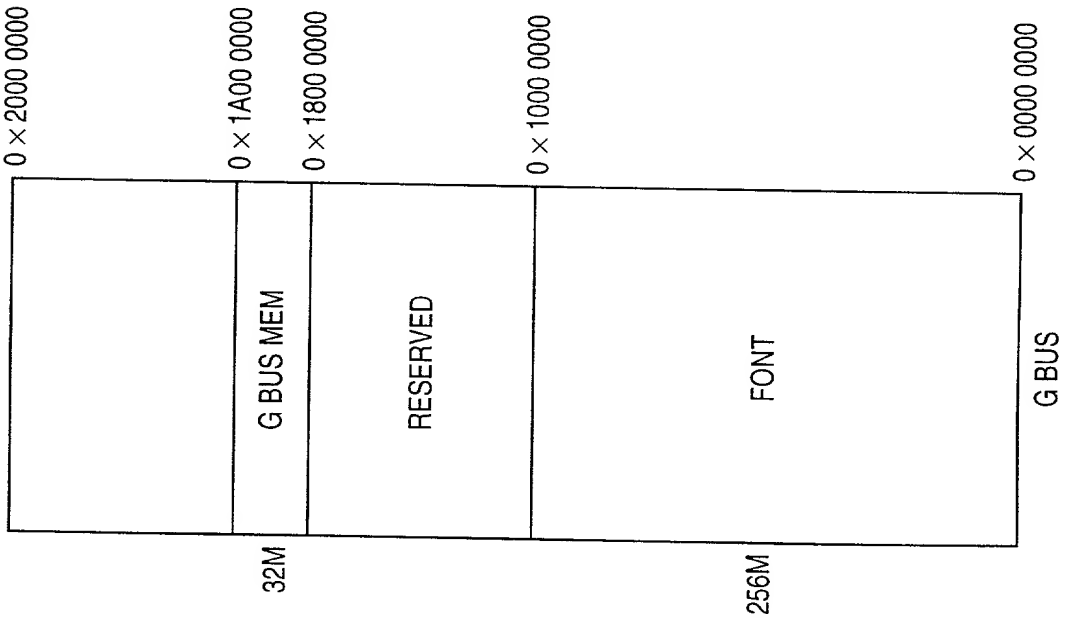


FIG. 24D

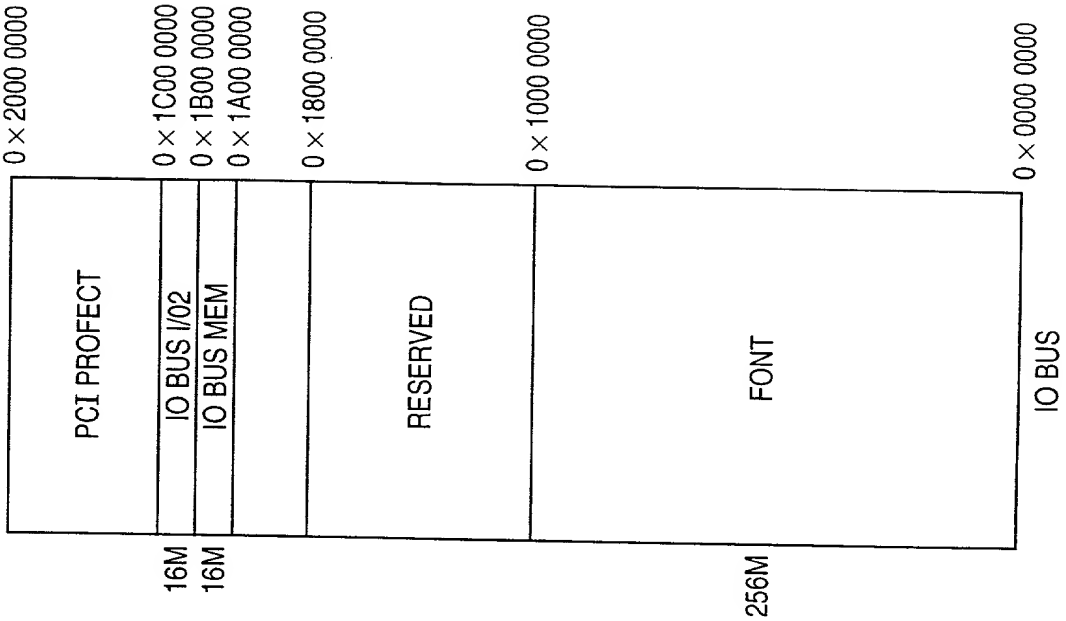


FIG. 25

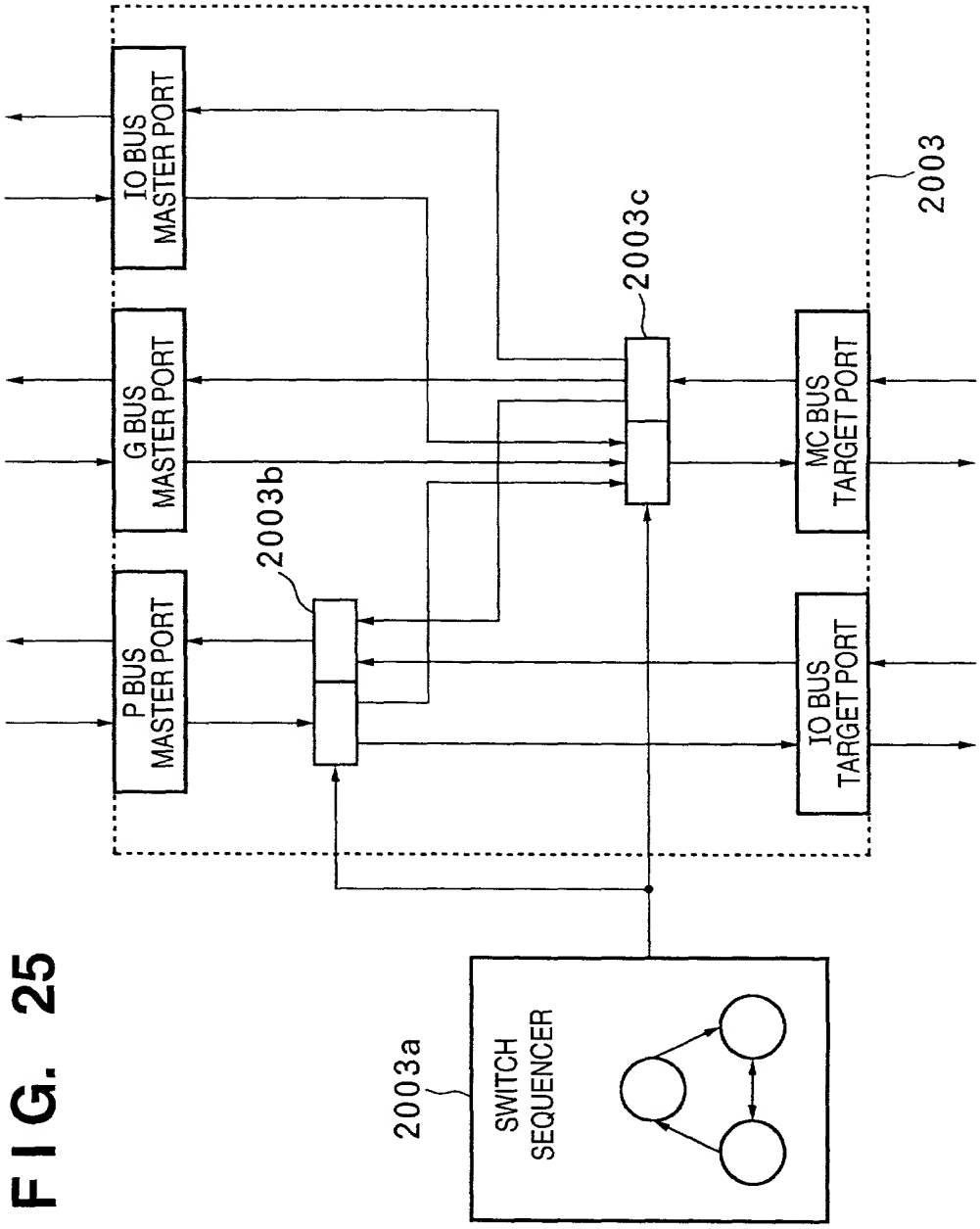
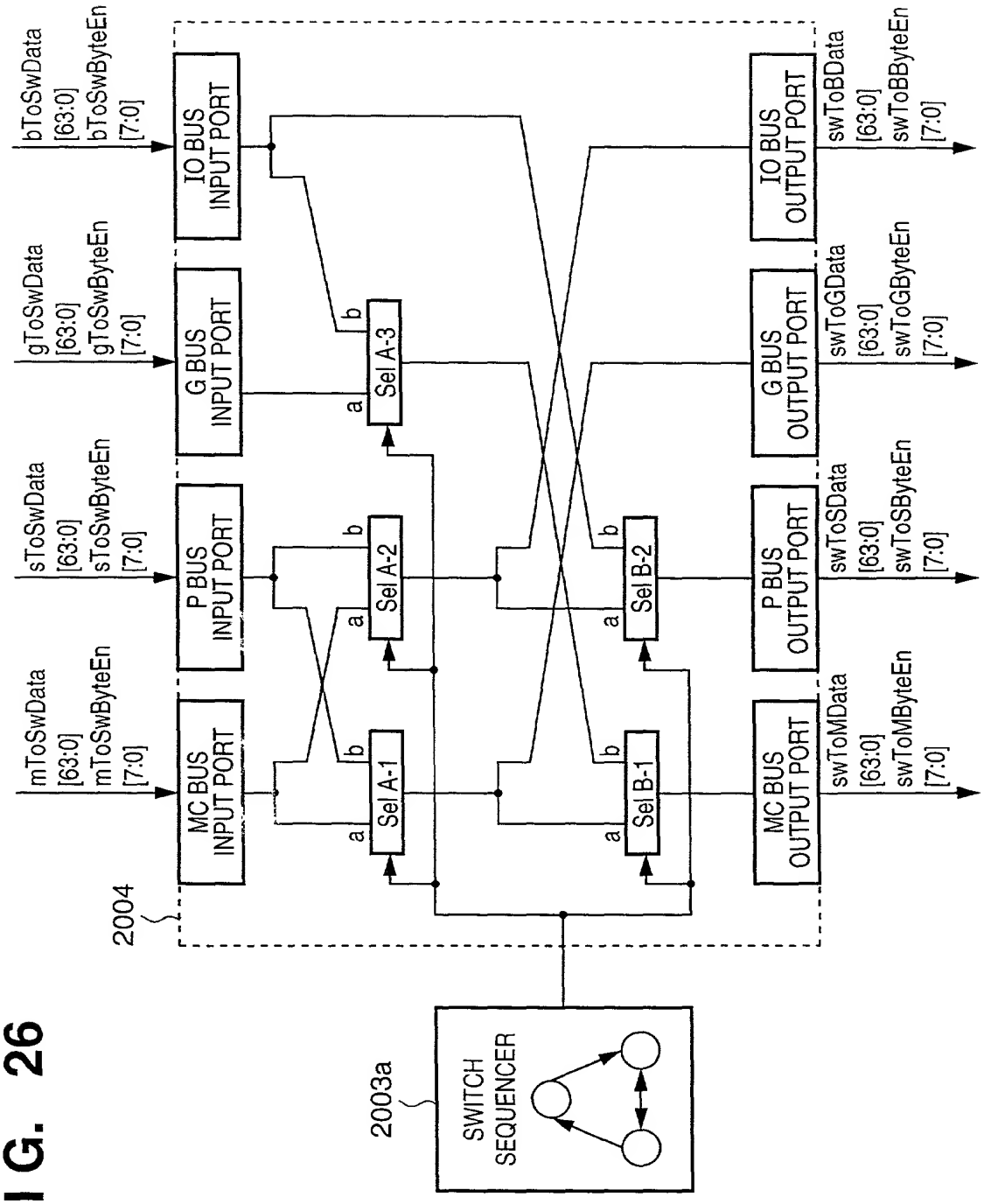

IO BUS MASTER PORT
G BUS MASTER PORT
P BUS MASTER PORT
2003b
2003c
MC BUS TARGET PORT
IO BUS TARGET PORT
2003
2003a
SWITCH SEQUENCER

FIG. 26


2004
2003a
SWITCH SEQUENCER
MC BUS INPUT PORT
P BUS INPUT PORT
G BUS INPUT PORT
IO BUS INPUT PORT
MC BUS OUTPUT PORT
P BUS OUTPUT PORT
G BUS OUTPUT PORT
IO BUS OUTPUT PORT
Sel A-1
Sel A-2
Sel A-3
Sel B-1
Sel B-2
mToSwData [63:0]
mToSwByteEn [7:0]
sToSwData [63:0]
sToSwByteEn [7:0]
gToSwData [63:0]
gToSwByteEn [7:0]
bToSwData [63:0]
bToSwByteEn [7:0]
swToMData [63:0]
swToMByteEn [7:0]
swToSData [63:0]
swToSByteEn [7:0]
swToGData [63:0]
swToGByteEn [7:0]
swToBData [63:0]
swToBByteEn [7:0]

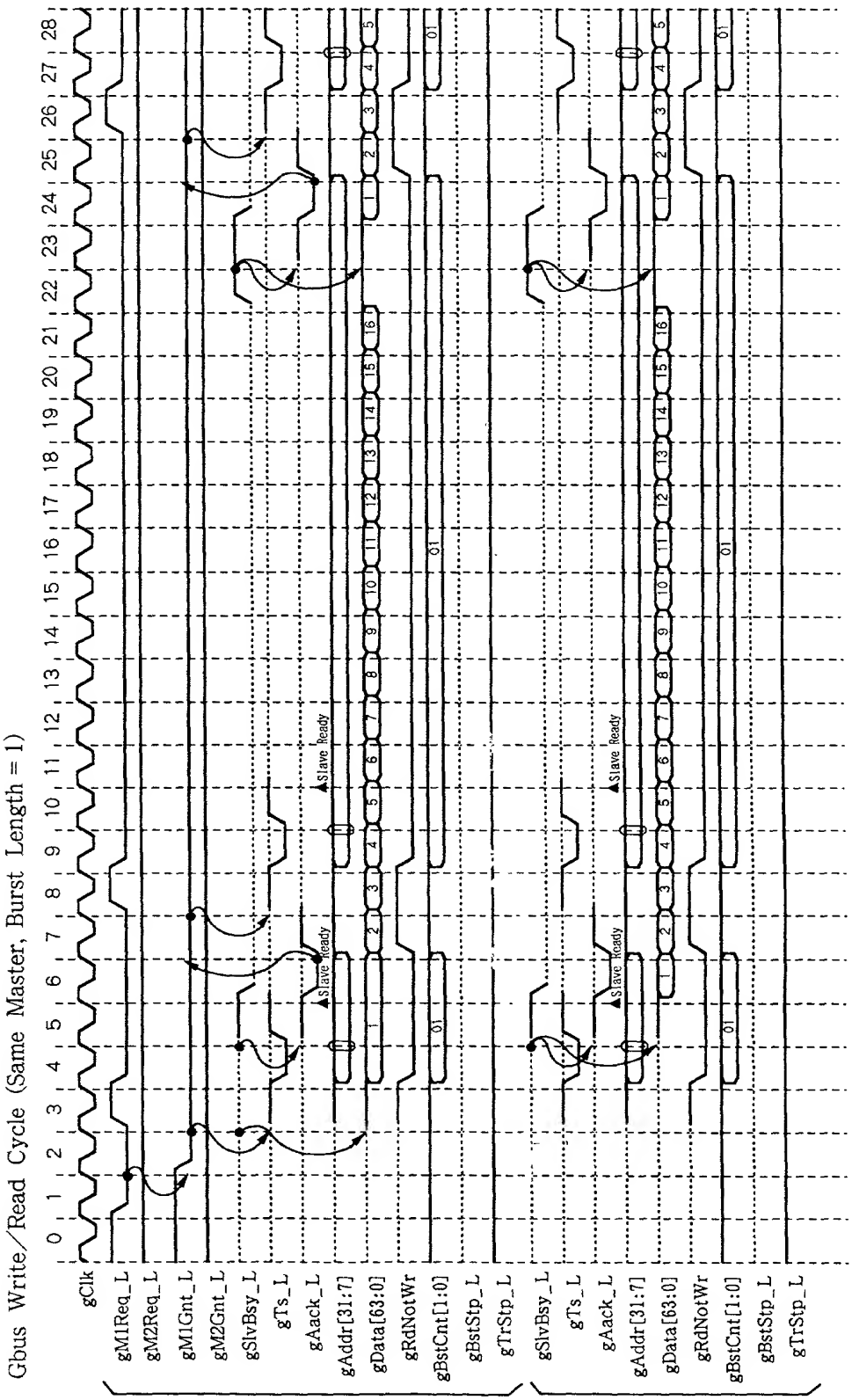

Gbus Write/Read Cycle (Same Master, Burst Length = 1)
WRITE CYCLE
READ CYCLE
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L
Slave Ready

FIG. 27

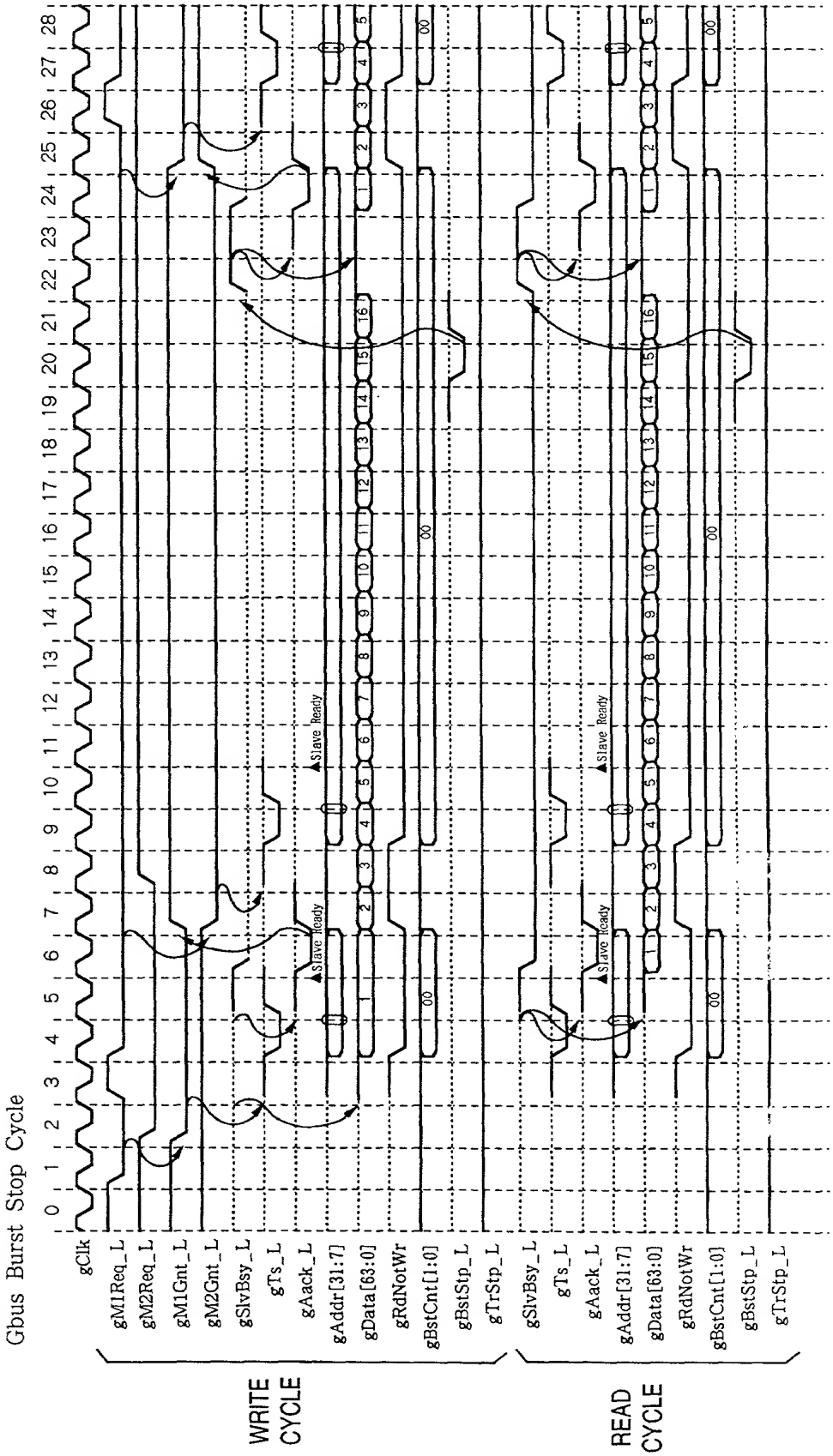

Gbus Burst Stop Cycle
WRITE CYCLE
READ CYCLE
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L
Slave Ready

FIG. 28

FIG. 29

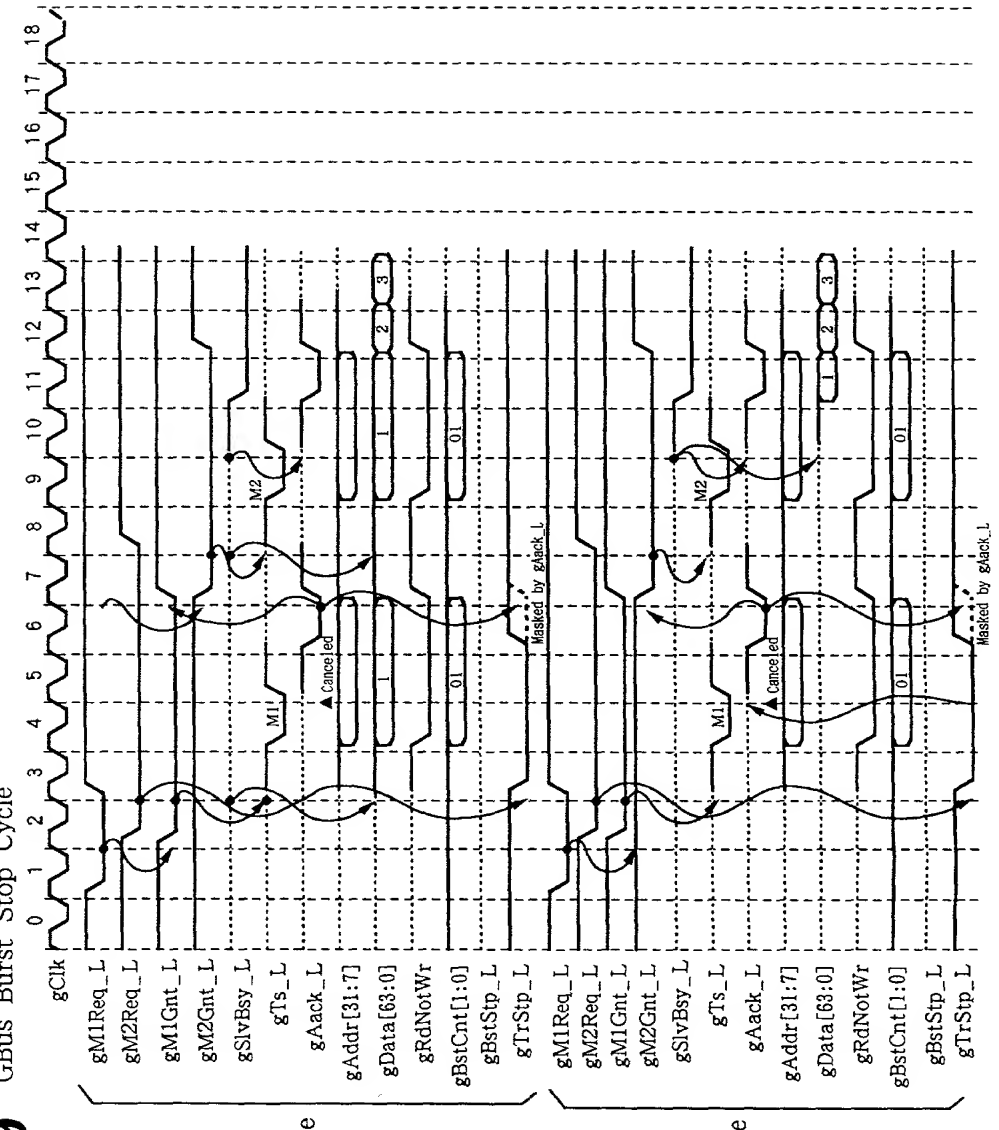

GBus Burst Stop Cycle
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L
Write Cycle
Read Cycle
M1
M2
Canceled
Masked by gAack_L

FIG. 30

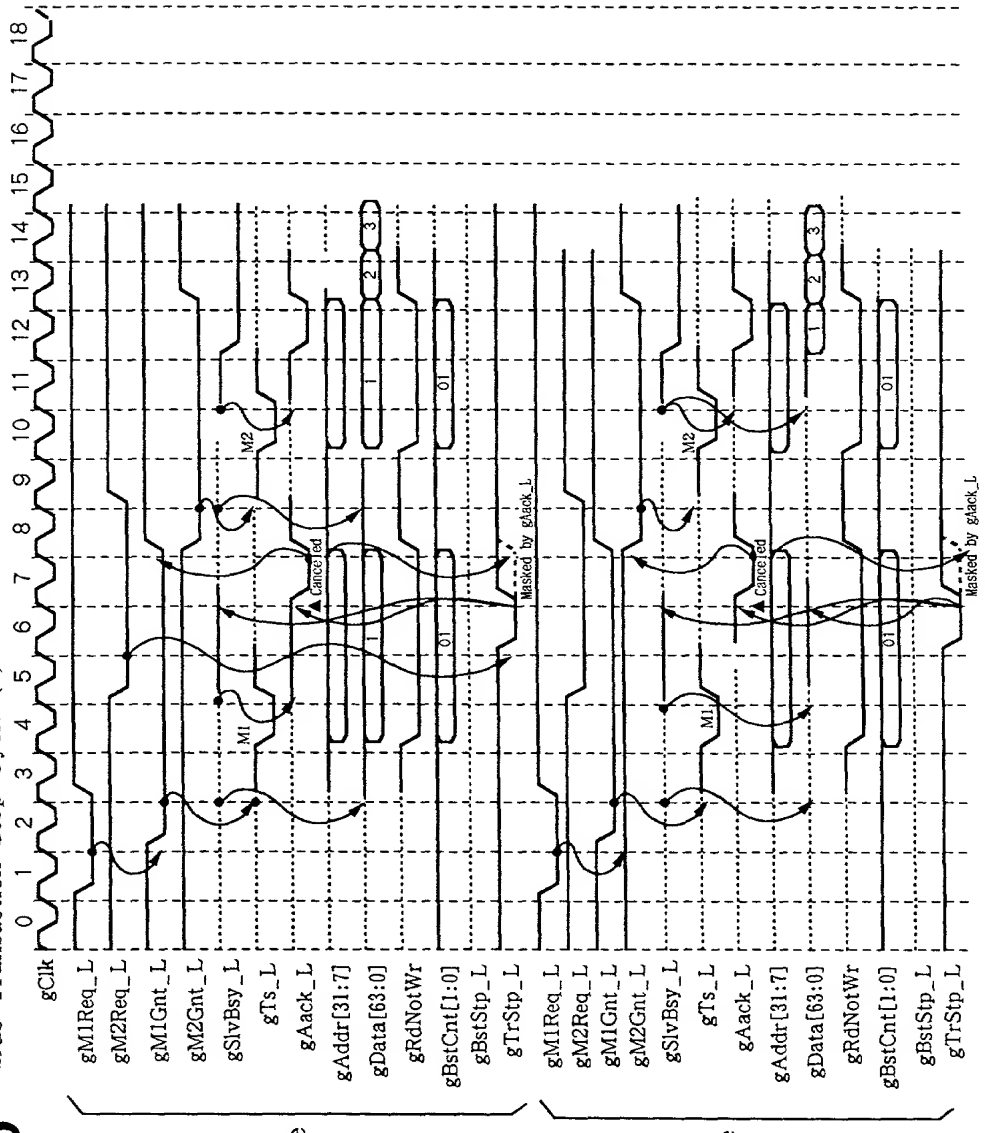

Bus Transaction Stop Cycle (2)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L
Write Cycle
M1
M2
Canceled
Masked by gAack_L
Read Cycle

FIG. 31

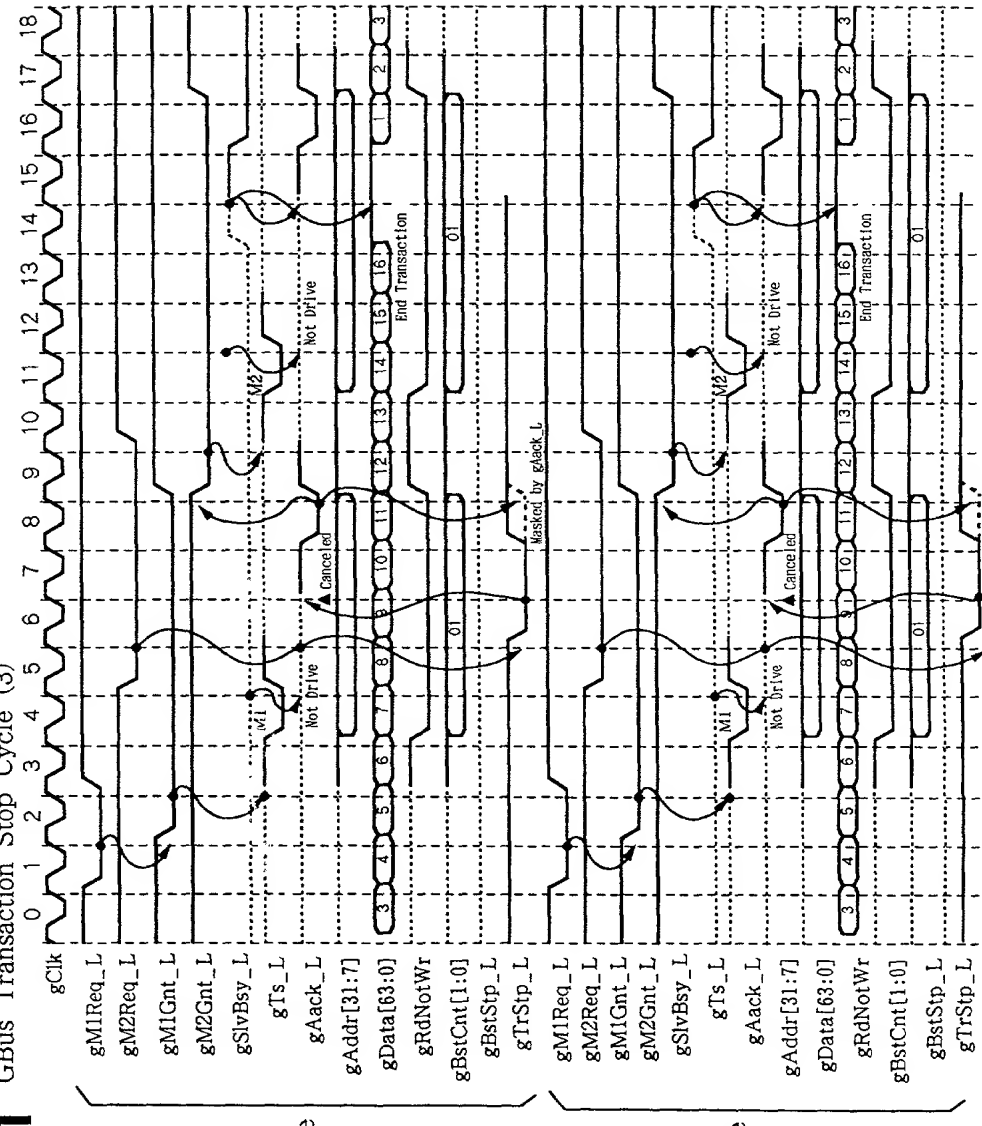
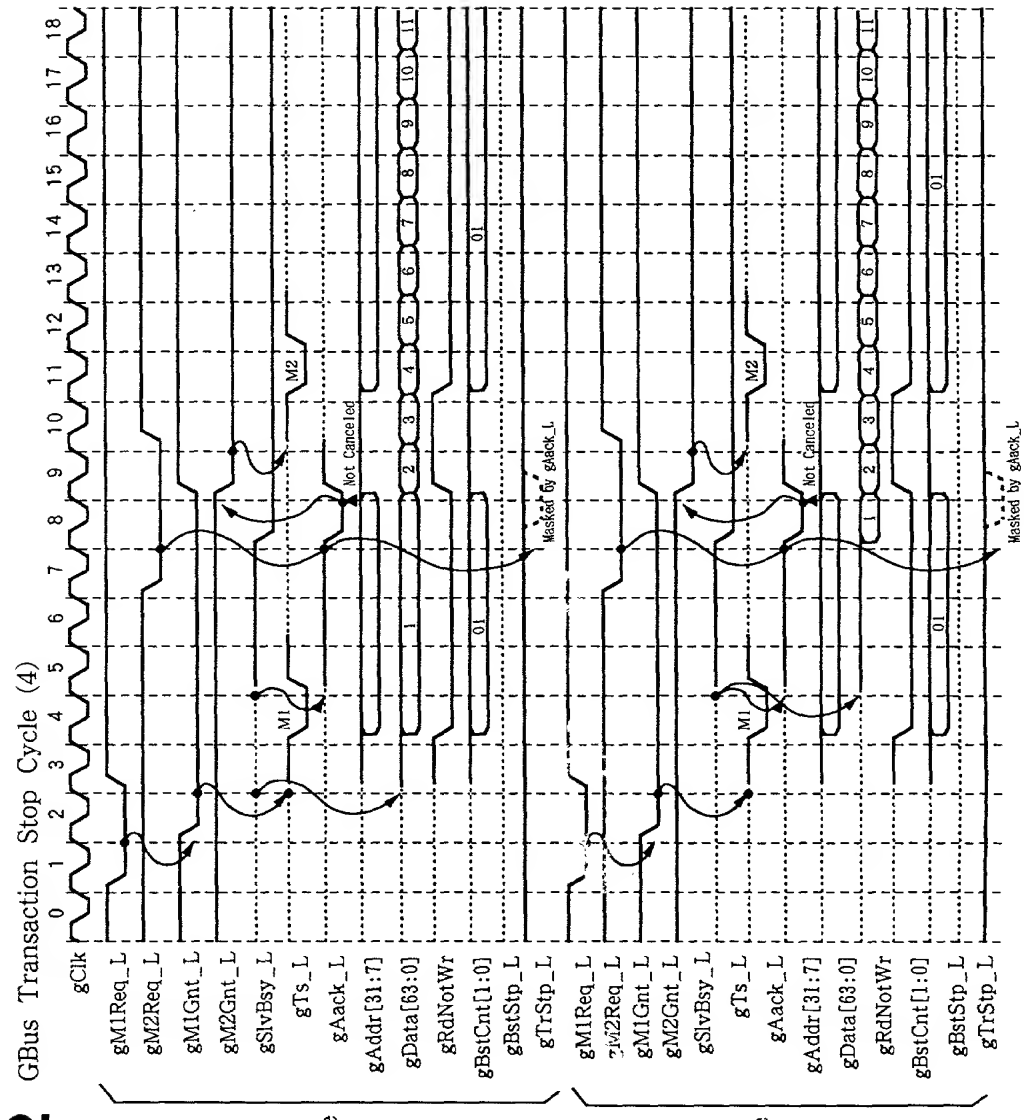

GBus Transaction Stop Cycle (3)
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L
Write Cycle
Read Cycle
M1
M2
Not Drive
Canceled
End Transaction
Masked by gAack_L

FIG. 32


GBus Transaction Stop Cycle (4)
Write Cycle
Read Cycle
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L
M1
M2
Not Canceled
Masked by gAack_L

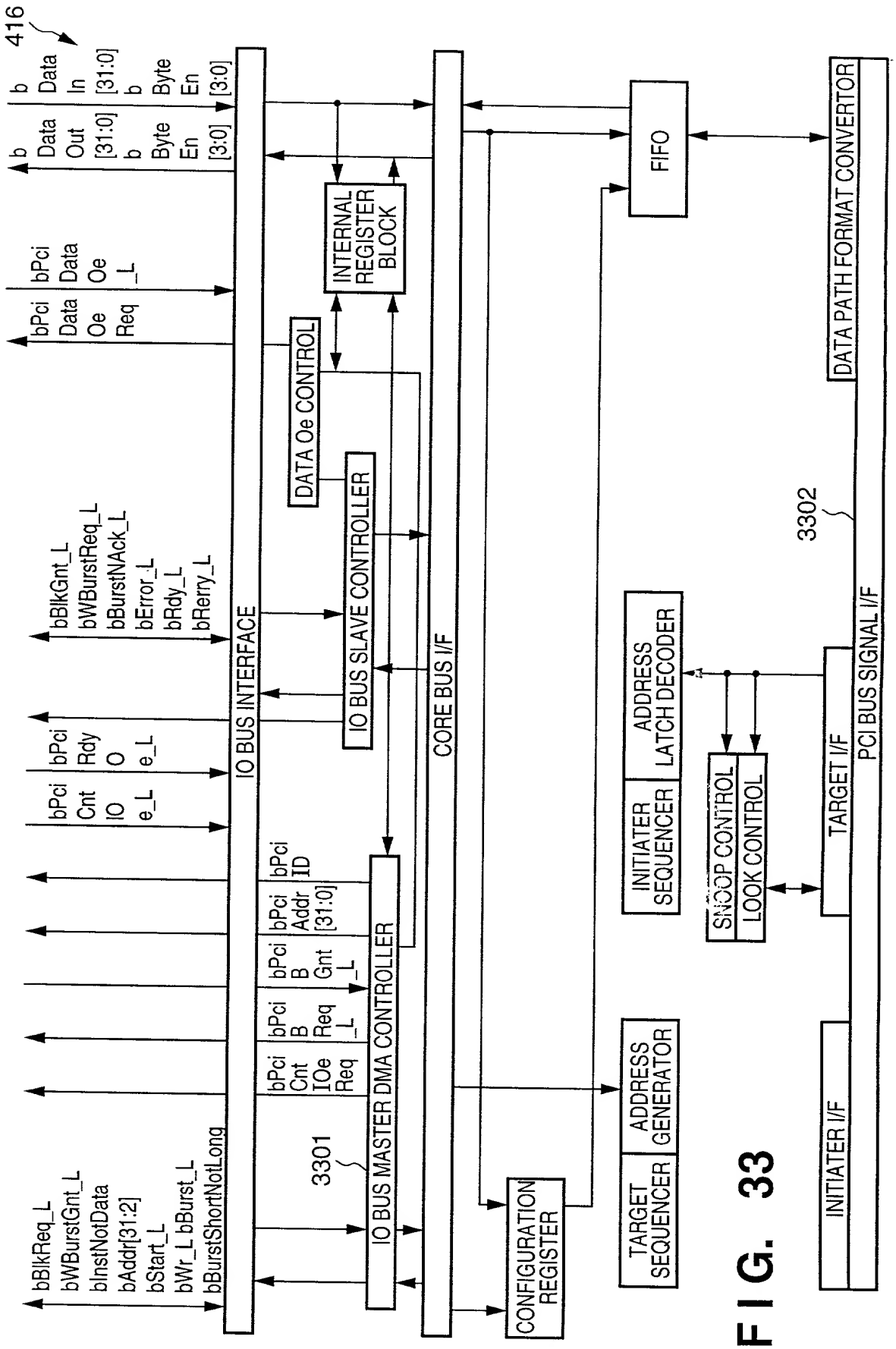
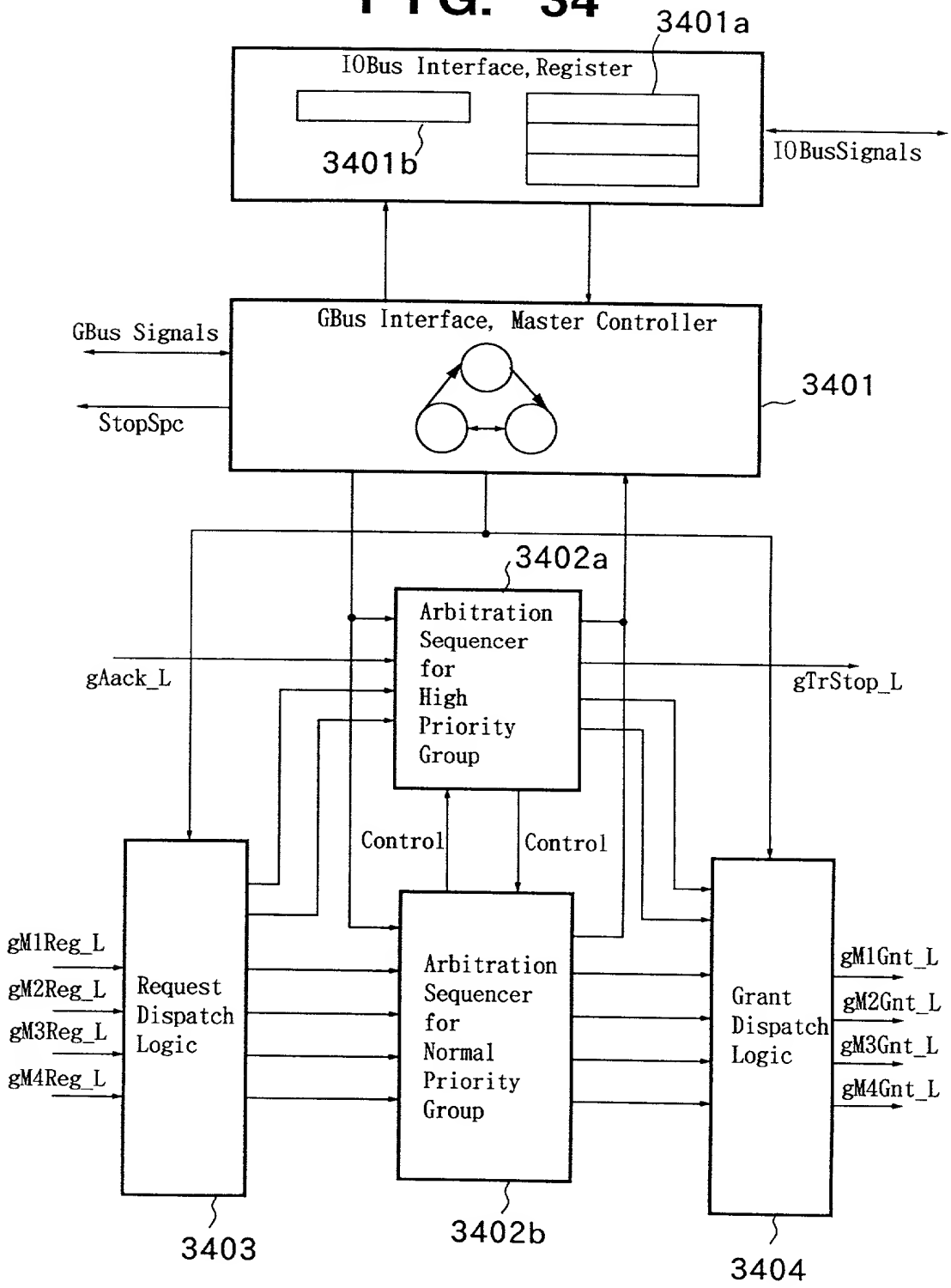

416
b Data In [31:0]
b Byte En [3:0]
b Data Out [31:0]
b Byte En [3:0]
bPci Data Oe _L
bPci Data Oe Req
bBlkGnt_L
bWBurstReq_L
bBurstNAck_L
bError_L
bRdy_L
bRerry_L
bPci Rdy O e_L
bPci Cnt IO e_L
bPci ID
bPci Addr [31:0]
bPci B Gnt _L
bPci B Req _L
bPci Cnt IOe Req
bBlkReq_L
bWBurstGnt_L
bInstNotData
bAddr[31:2]
bStart_L
bWr_L bBurst_L
bBurstShortNotLong
IO BUS INTERFACE
DATA Oe CONTROL
INTERNAL REGISTER BLOCK
IO BUS SLAVE CONTROLLER
IO BUS MASTER DMA CONTROLLER
3301
CORE BUS I/F
FIFO
DATA PATH FORMAT CONVERTOR
3302
INITIATER SEQUENCER
ADDRESS LATCH DECODER
SNOOP CONTROL
LOOK CONTROL
CONFIGURATION REGISTER
TARGET SEQUENCER
ADDRESS GENERATOR
TARGET I/F
INITIATER I/F
PCI BUS SIGNAL I/F

FIG. 33

FIG. 34


3401a
IOBus Interface, Register
3401b
IOBusSignals
GBus Interface, Master Controller
GBus Signals
StopSpc
3401
3402a
Arbitration Sequencer for High Priority Group
gAack_L
gTrStop_L
Control
Control
gM1Reg_L
gM2Reg_L
gM3Reg_L
gM4Reg_L
Request Dispatch Logic
Arbitration Sequencer for Normal Priority Group
Grant Dispatch Logic
gM1Gnt_L
gM2Gnt_L
gM3Gnt_L
gM4Gnt_L
3403
3402b
3404

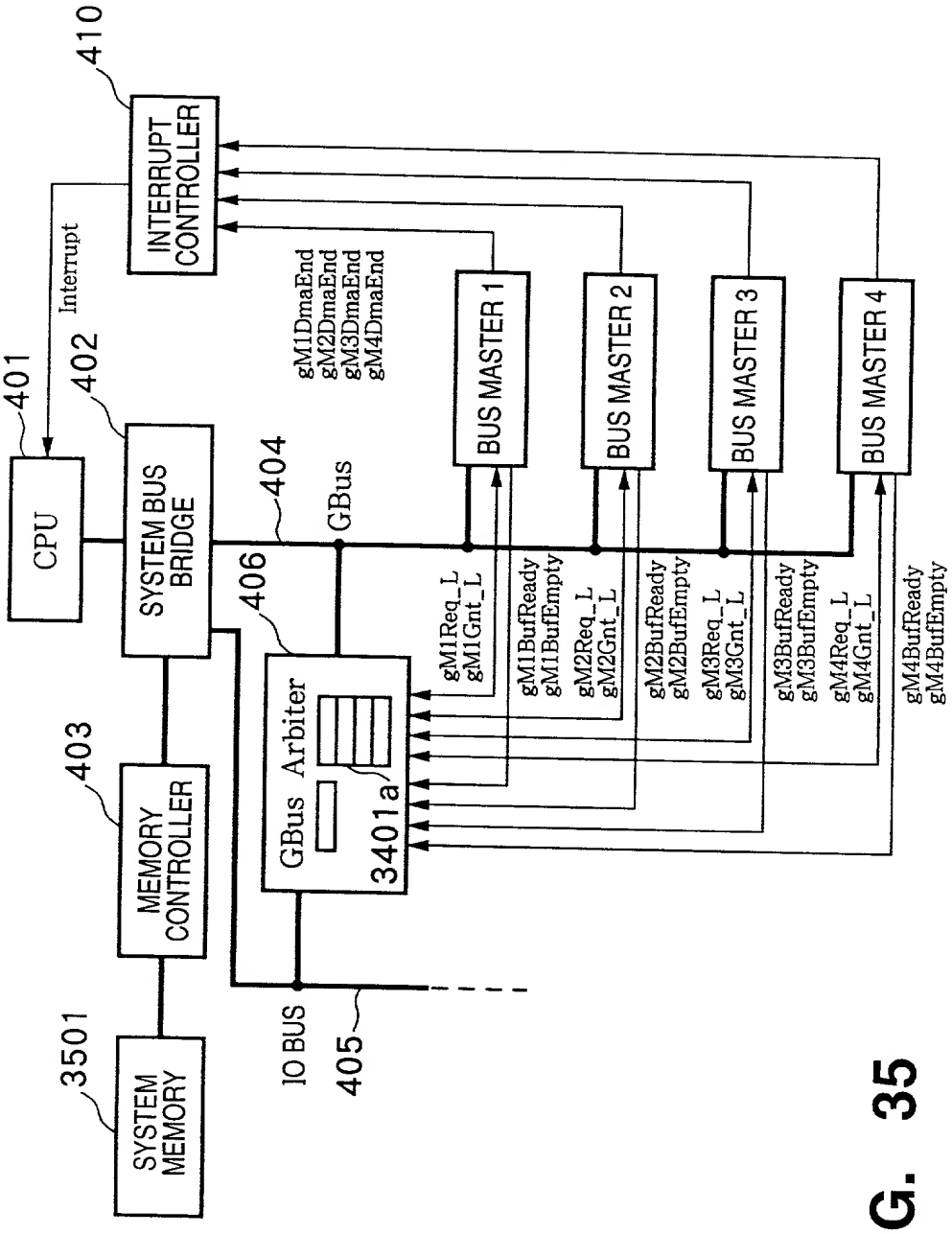

410
INTERRUPT CONTROLLER
Interrupt
401
CPU
402
SYSTEM BUS BRIDGE
404
GBus
406
GBus Arbiter
3401a
403
MEMORY CONTROLLER
3501
SYSTEM MEMORY
IO BUS
405
gM1DmaEnd
gM2DmaEnd
gM3DmaEnd
gM4DmaEnd
BUS MASTER 1
BUS MASTER 2
BUS MASTER 3
BUS MASTER 4
gM1Req_L
gM1Gnt_L
gM1BufReady
gM1BufEmpty
gM2Req_L
gM2Gnt_L
gM2BufReady
gM2BufEmpty
gM3Req_L
gM3Gnt_L
gM3BufReady
gM3BufEmpty
gM4Req_L
gM4Gnt_L
gM4BufReady
gM4BufEmpty

FIG. 35

FIG. 36

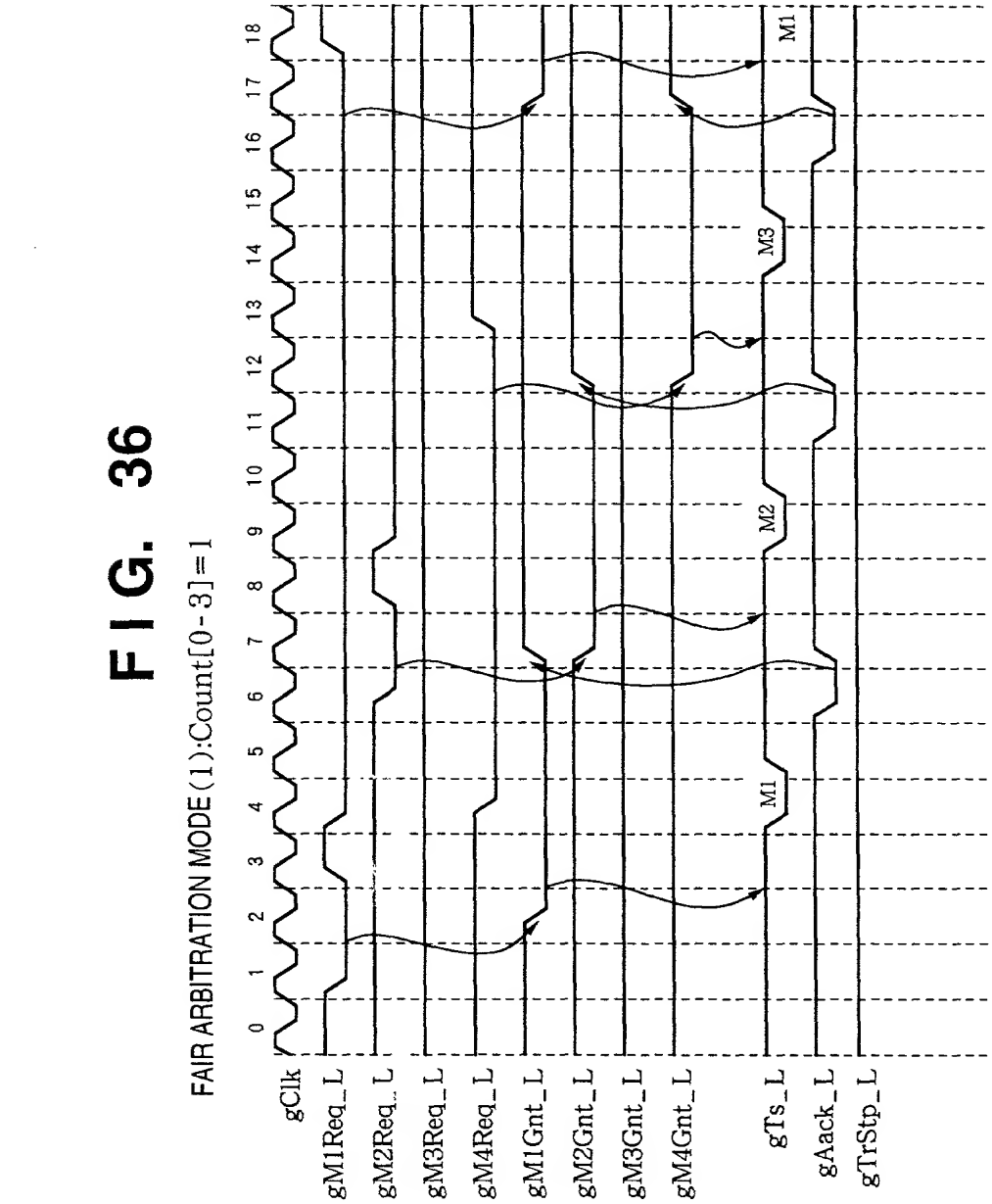

FAIR ARBITRATION MODE(1):Count[0-3]=1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
gClk
gM1Req_L
gM2Req_L
gM3Req_L
gM4Req_L
gM1Gnt_L
gM2Gnt_L
gM3Gnt_L
gM4Gnt_L
gTs_L
gAack_L
gTrStp_L
M1
M2
M3
M1

FIG. 37

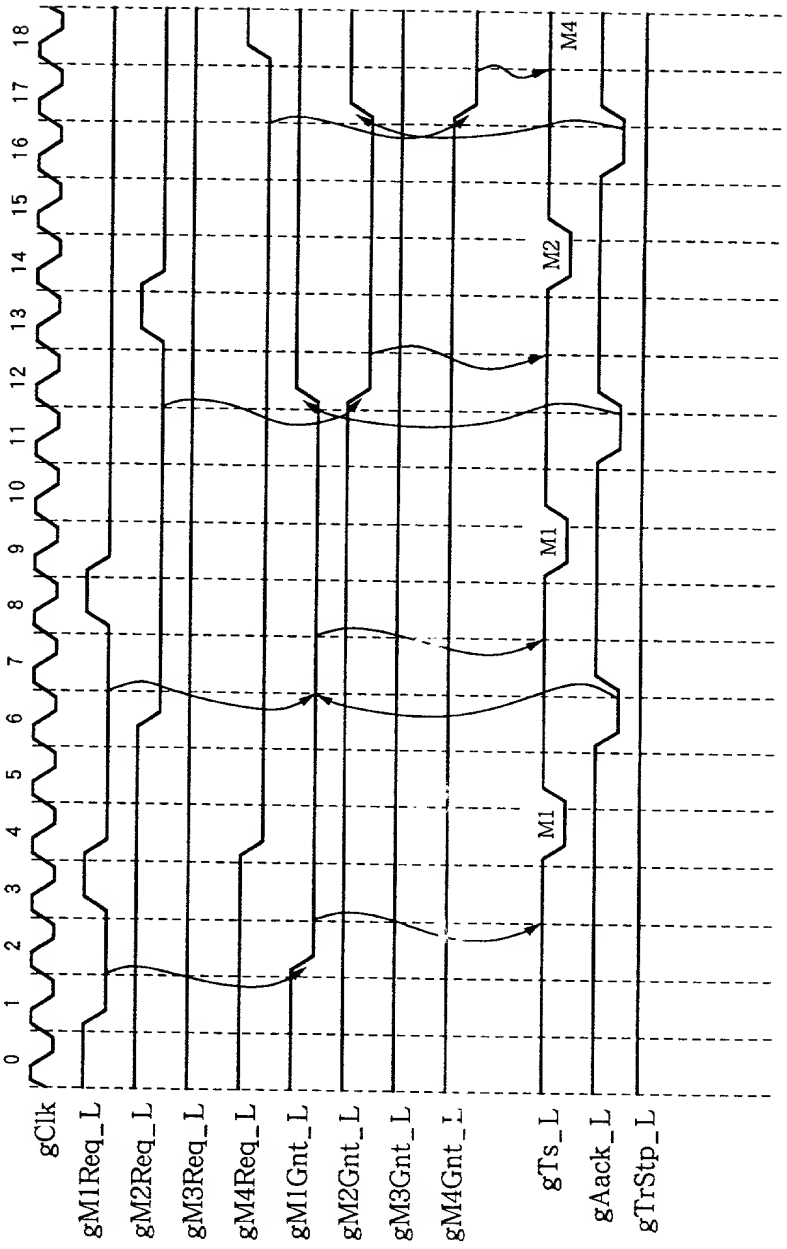

FAIR ARBITRATION MODE (2):Count[0]=2,Count[1-3]=1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
gClk
gM1Req_L
gM2Req_L
gM3Req_L
gM4Req_L
gM1Gnt_L
gM2Gnt_L
gM3Gnt_L
gM4Gnt_L
gTs_L
gAack_L
gTrStp_L
M1
M1
M2
M4

FIG. 38

HIGH-PRIORITY ARBITRATION MODE (1):High Priority Bus Master=[0],Count[0-3]=1

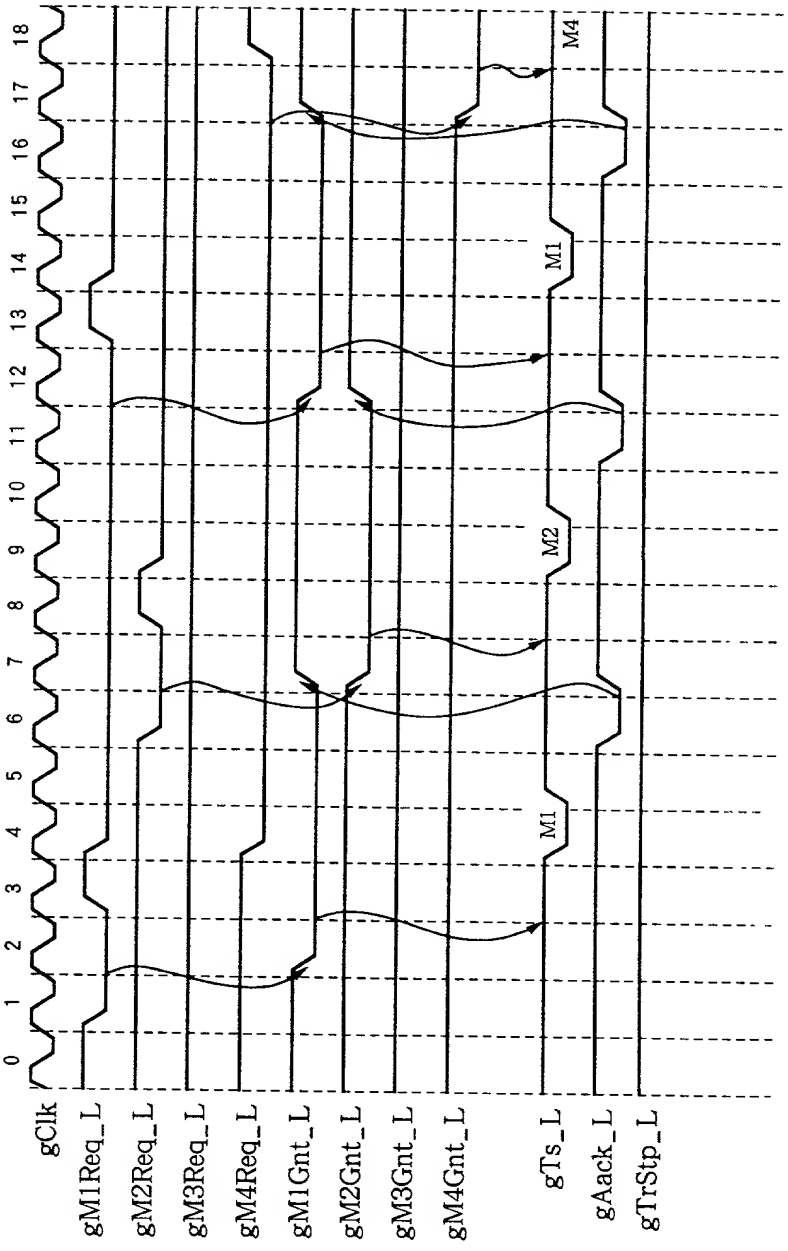


FIG. 39

TRANSACTION STOP CYCLE (1):High Priority Bus Master=[0]

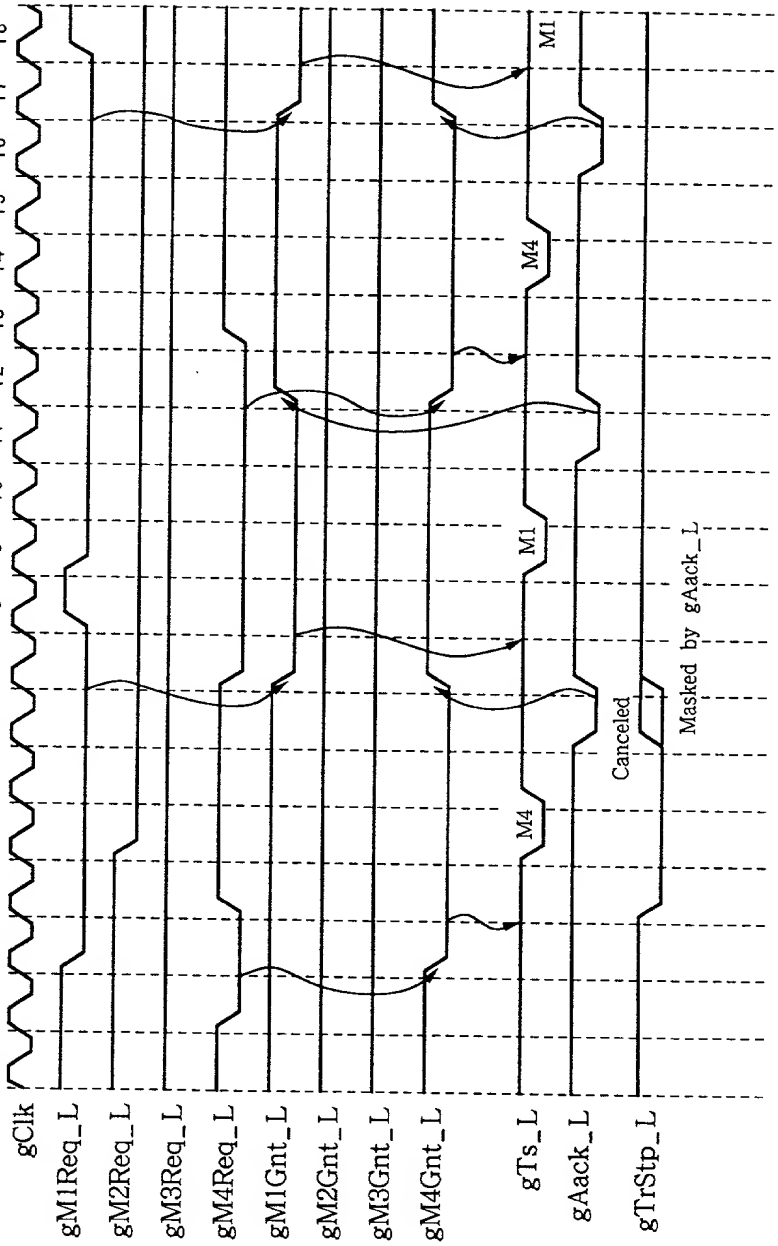
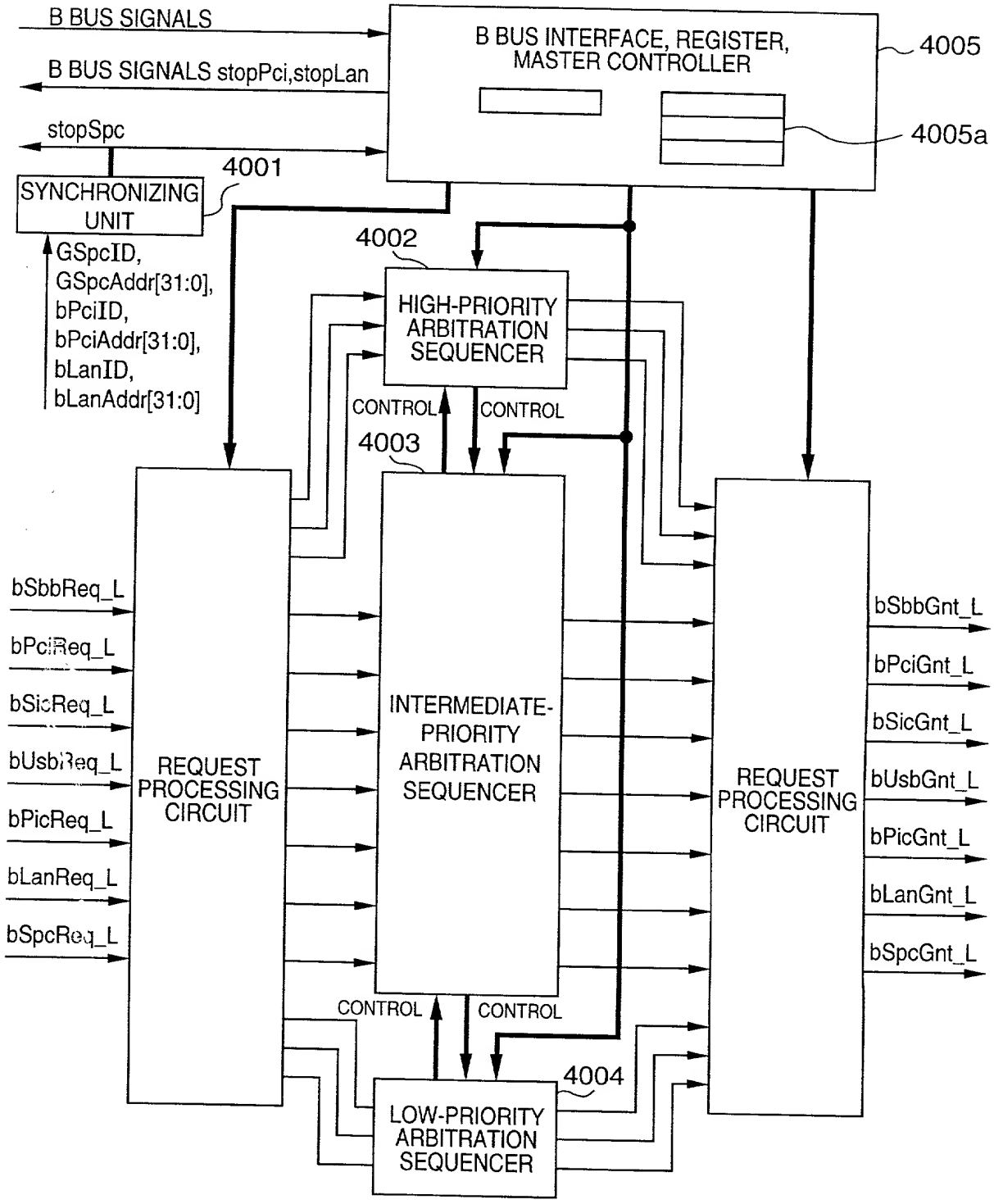


FIG. 40


B BUS SIGNALS
B BUS SIGNALS stopPci,stopLan
stopSpc
B BUS INTERFACE, REGISTER, MASTER CONTROLLER
4005
4005a
4001
SYNCHRONIZING UNIT
GSpcID,
GSpcAddr[31:0],
bPciID,
bPciAddr[31:0],
bLanID,
bLanAddr[31:0]
4002
HIGH-PRIORITY ARBITRATION SEQUENCER
CONTROL
CONTROL
4003
bSbbReq_L
bPciReq_L
bSicReq_L
bUsbReq_L
bPicReq_L
bLanReq_L
bSpcReq_L
REQUEST PROCESSING CIRCUIT
INTERMEDIATE-PRIORITY ARBITRATION SEQUENCER
REQUEST PROCESSING CIRCUIT
bSbbGnt_L
bPciGnt_L
bSicGnt_L
bUsbGnt_L
bPicGnt_L
bLanGnt_L
bSpcGnt_L
CONTROL
CONTROL
4004
LOW-PRIORITY ARBITRATION SEQUENCER

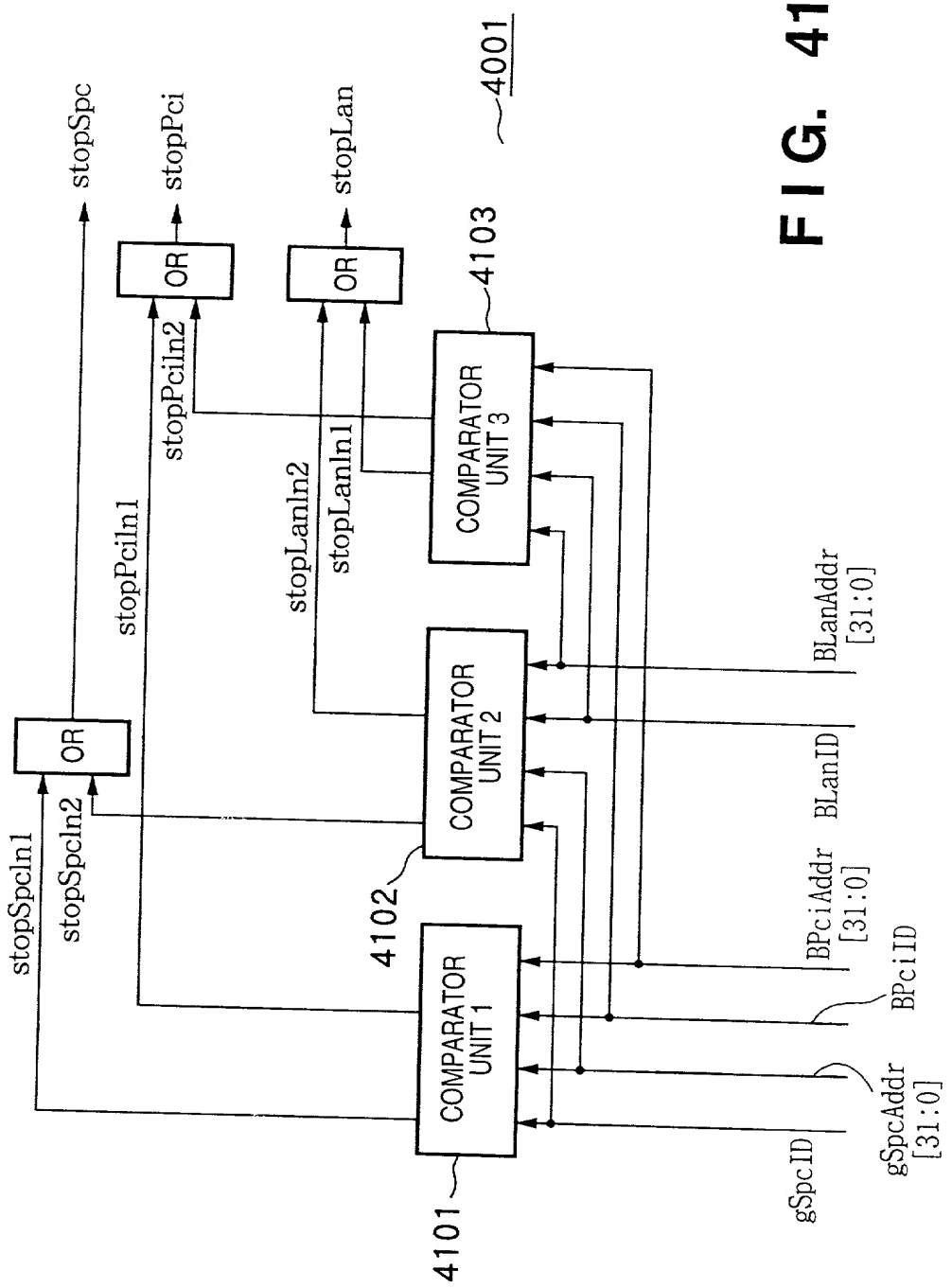

4001
4101
4102
4103
COMPARATOR UNIT 1
COMPARATOR UNIT 2
COMPARATOR UNIT 3
OR
OR
OR
stopSpc
stopPci
stopLan
stopSpcIn1
stopSpcIn2
stopPciIn1
stopPciIn2
stopLanIn1
stopLanIn2
gSpcID
gSpcAddr [31:0]
BPciID
BPciAddr [31:0]
BLanID
BLanAddr [31:0]

FIG. 41

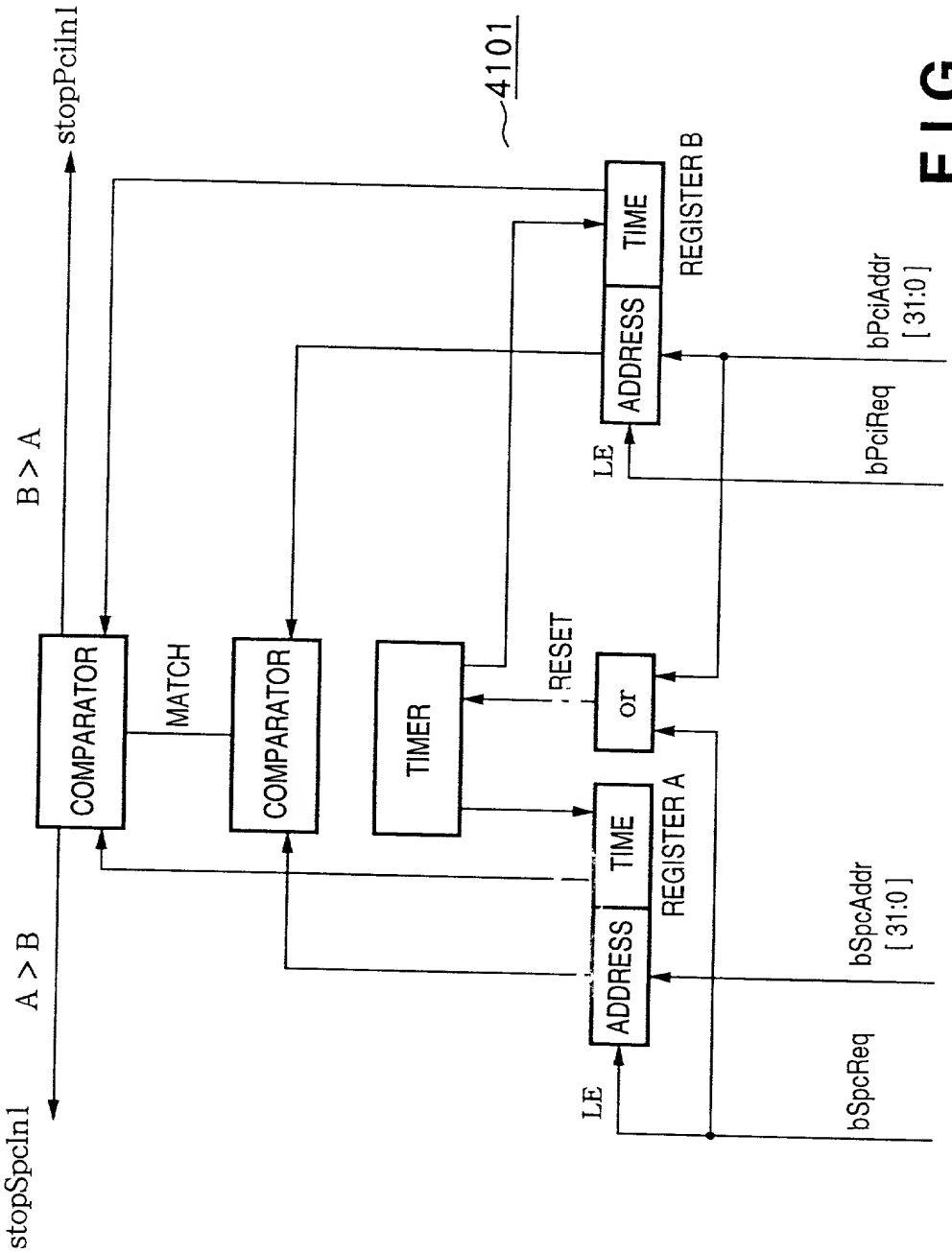
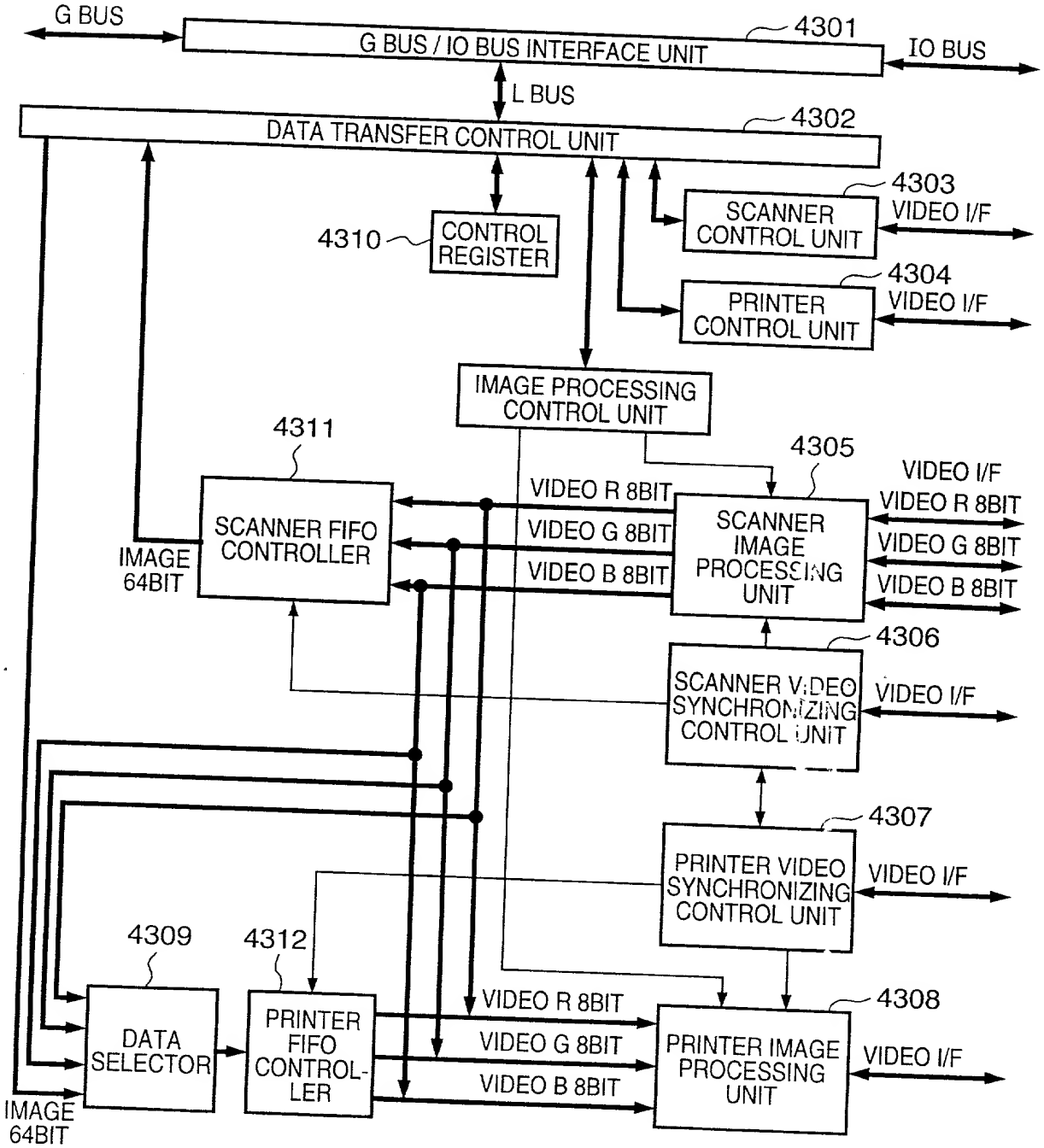

stopPciIn1
4101
B > A
COMPARATOR
MATCH
COMPARATOR
TIMER
RESET
or
REGISTER B
TIME
ADDRESS
LE
bPciAddr
[31:0]
bPciReq
REGISTER A
TIME
ADDRESS
LE
bSpcAddr
[31:0]
bSpcReq
A > B
stopSpcIn1

FIG. 42

FIG. 43


G BUS
G BUS / IO BUS INTERFACE UNIT
4301
IO BUS
L BUS
DATA TRANSFER CONTROL UNIT
4302
4303
SCANNER CONTROL UNIT
VIDEO I/F
4310
CONTROL REGISTER
4304
PRINTER CONTROL UNIT
VIDEO I/F
IMAGE PROCESSING CONTROL UNIT
4311
4305
VIDEO I/F
VIDEO R 8BIT
VIDEO R 8BIT
SCANNER FIFO CONTROLLER
VIDEO G 8BIT
SCANNER IMAGE PROCESSING UNIT
VIDEO G 8BIT
IMAGE 64BIT
VIDEO B 8BIT
VIDEO B 8BIT
4306
SCANNER VIDEO SYNCHRONIZING CONTROL UNIT
VIDEO I/F
4307
PRINTER VIDEO SYNCHRONIZING CONTROL UNIT
VIDEO I/F
4309
4312
VIDEO R 8BIT
4308
DATA SELECTOR
PRINTER FIFO CONTROL-LER
VIDEO G 8BIT
PRINTER IMAGE PROCESSING UNIT
VIDEO I/F
VIDEO B 8BIT
IMAGE 64BIT

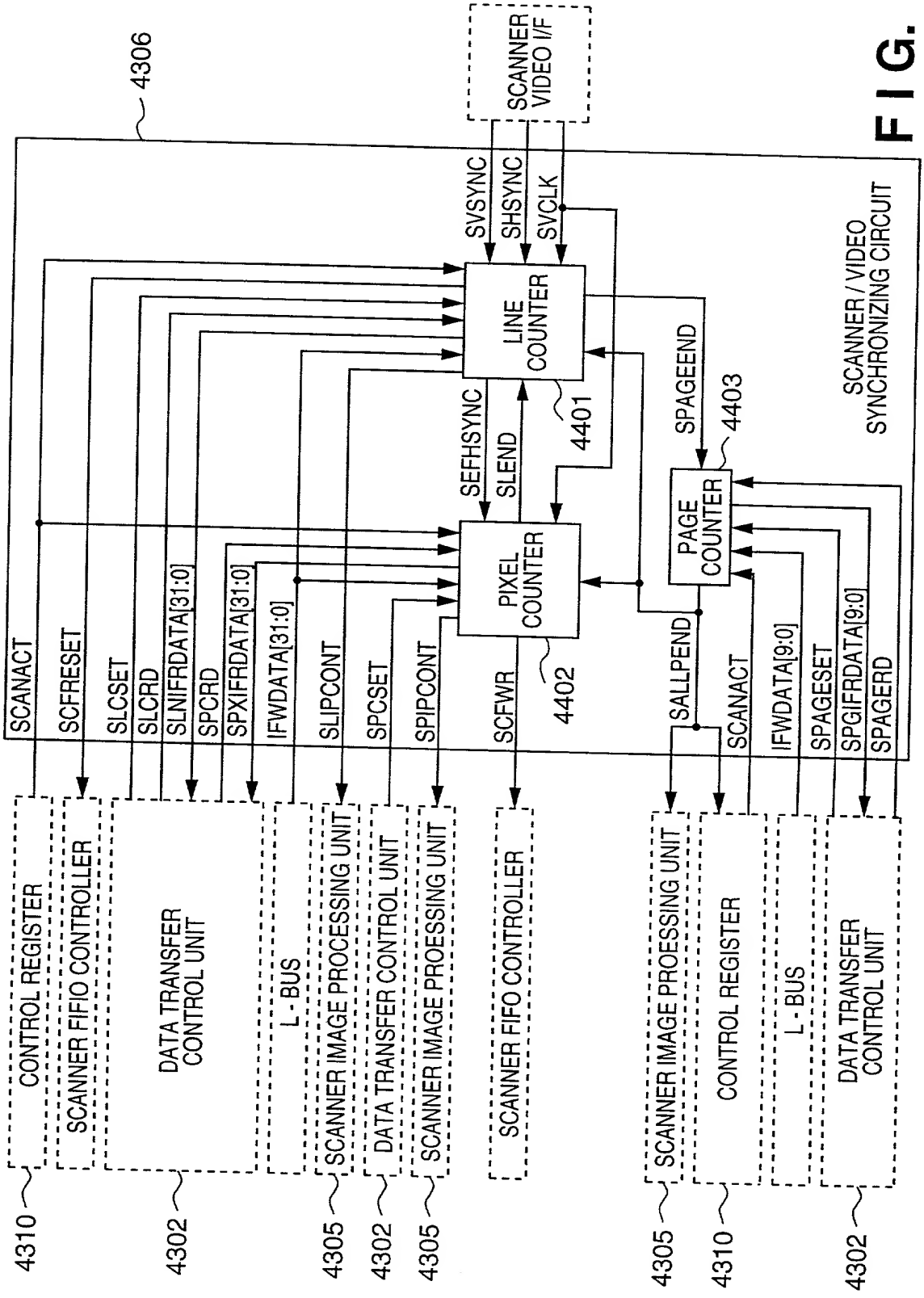

4306
SCANNER VIDEO I/F
SVSYNC
SHSYNC
SVCLK
LINE COUNTER
4401
SEFHSYNC
SLEND
SPAGEEND
4403
PAGE COUNTER
PIXEL COUNTER
4402
SCANNER / VIDEO SYNCHRONIZING CIRCUIT
SCANACT
SCFRESET
SLCSET
SLCRD
SLNIFRDATA[31:0]
SPCRD
SPXIFRDATA[31:0]
IFWDATA[31:0]
SLIPCONT
SPCSET
SPIPCONT
SCFWR
SALLPEND
SCANACT
IFWDATA[9:0]
SPAGESET
SPGIFRDATA[9:0]
SPAGERD
CONTROL REGISTER
SCANNER FIFIO CONTROLLER
DATA TRANSFER CONTROL UNIT
L - BUS
SCANNER IMAGE PROCESSING UNIT
DATA TRANSFER CONTROL UNIT
SCANNER IMAGE PROESSING UNIT
SCANNER FIFO CONTROLLER
SCANNER IMAGE PROESSING UNIT
CONTROL REGISTER
L - BUS
DATA TRANSFER CONTROL UNIT
4310
4302
4305
4302
4305
4305
4310
4302

FIG. 44

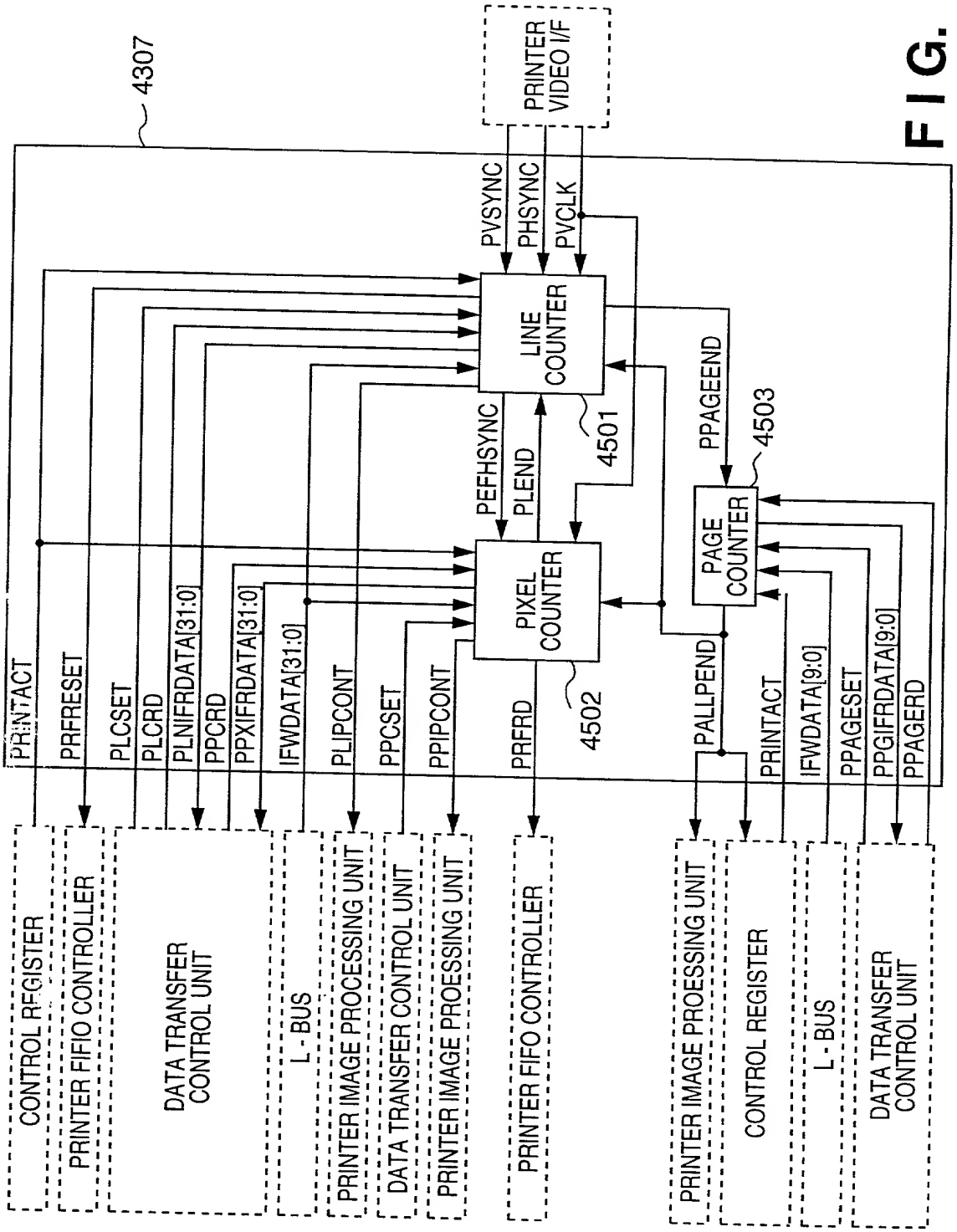
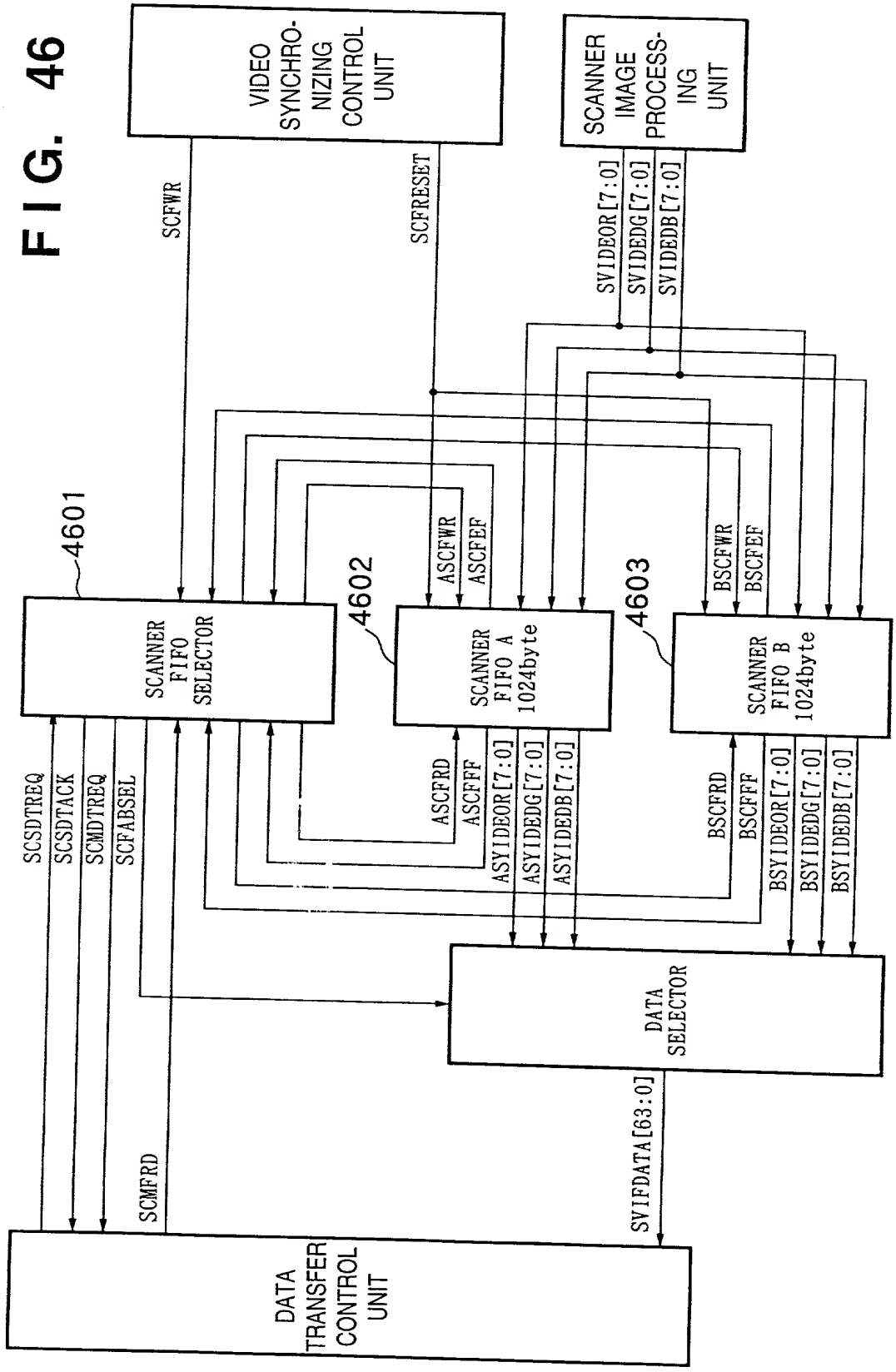

4307
PRINTER VIDEO I/F
PVSYNC
PHSYNC
PVCLK
LINE COUNTER
4501
PEFHSYNC
PLEND
PPAGEEND
4503
PAGE COUNTER
PIXEL COUNTER
4502
PRINTACT
PRFRESET
PLCSET
PLCRD
PLNIFRDATA[31:0]
PPCRD
PPXIFRDATA[31:0]
IFWDATA[31:0]
PLIPCONT
PPCSET
PPIPCONT
PRFRD
PALLPEND
PRINTACT
IFWDATA[9:0]
PPAGESET
PPGIFRDATA[9:0]
PPAGERD
CONTROL REGISTER
PRINTER FIFIO CONTROLLER
DATA TRANSFER CONTROL UNIT
L - BUS
PRINTER IMAGE PROCESSING UNIT
DATA TRANSFER CONTROL UNIT
PRINTER IMAGE PROESSING UNIT
PRINTER FIFO CONTROLLER
PRINTER IMAGE PROESSING UNIT
CONTROL REGISTER
L - BUS
DATA TRANSFER CONTROL UNIT

FIG. 45

FIG. 46


VIDEO SYNCHRO-NIZING CONTROL UNIT
SCANNER IMAGE PROCESS-ING UNIT
SCFWR
SCFRESET
SVIDEOR[7:0]
SVIDEDG[7:0]
SVIDEDB[7:0]
4601
SCANNER FIFO SELECTOR
4602
SCANNER FIFO A 1024byte
4603
SCANNER FIFO B 1024byte
ASCFWR
ASCFEF
BSCFWR
BSCFEF
SCSDTREQ
SCSDTACK
SCMDTREQ
SCFABSEL
ASCFRD
ASCFFF
ASYIDEOR[7:0]
ASYIDEDG[7:0]
ASYIDEDB[7:0]
BSCFRD
BSCFFF
BSYIDEOR[7:0]
BSYIDEDG[7:0]
BSYIDEDB[7:0]
DATA SELECTOR
SCMFRD
SVIFDATA[63:0]
DATA TRANSFER CONTROL UNIT

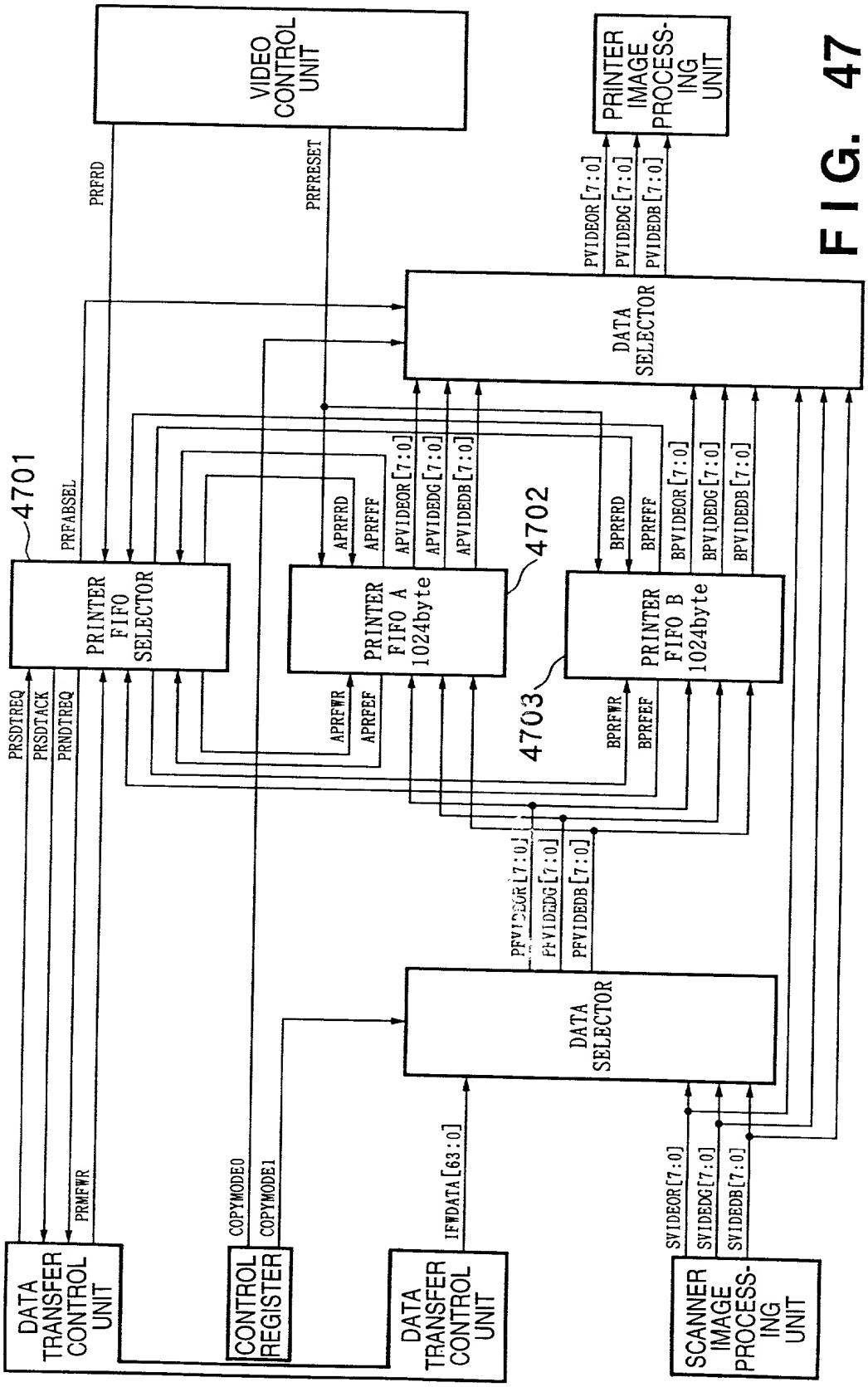
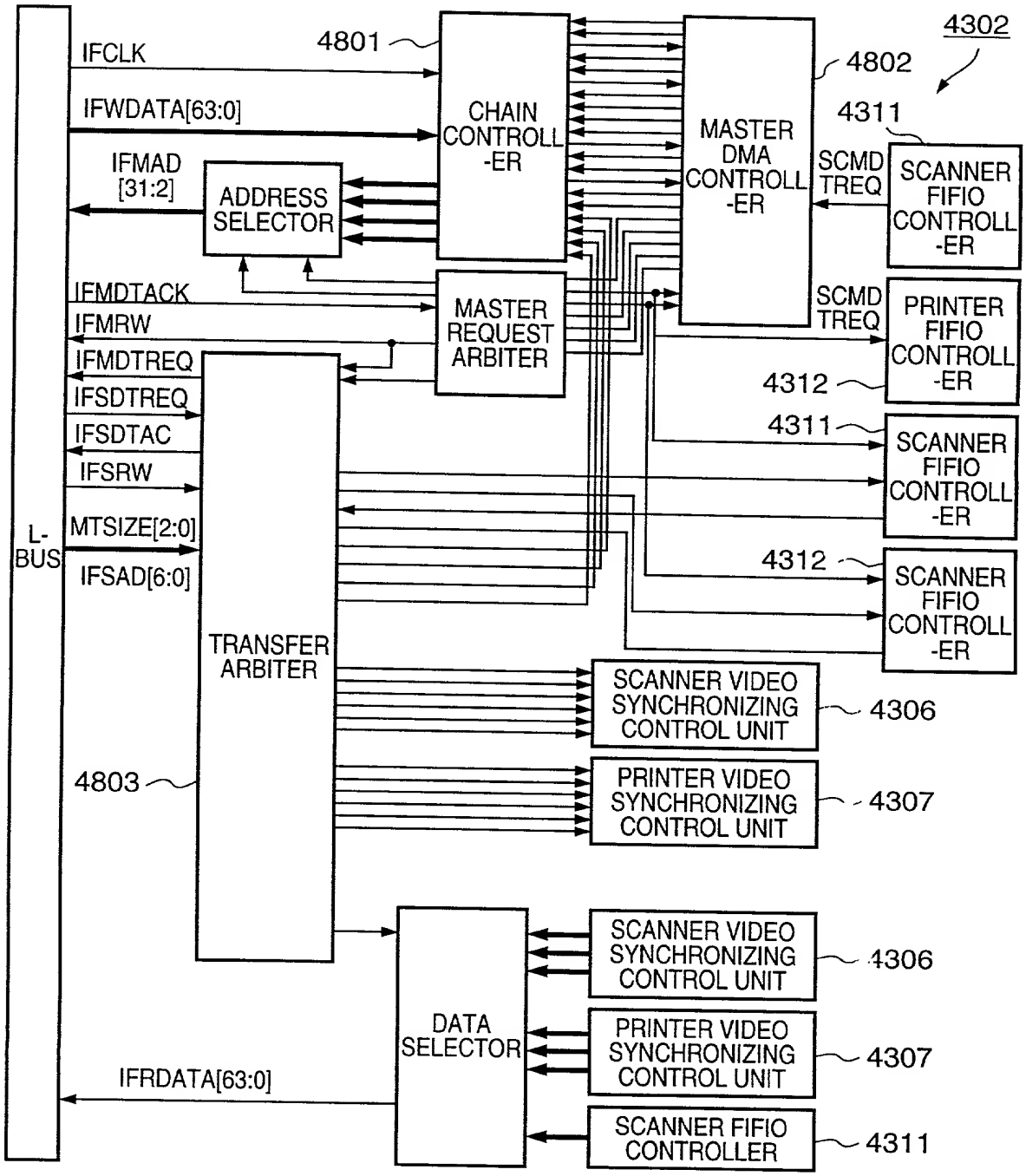

VIDEO CONTROL UNIT
PRINTER IMAGE PROCESS-ING UNIT
PRFRD
PRFRESET
PVIDEOR[7:0]
PVIDEDG[7:0]
PVIDEDB[7:0]
DATA SELECTOR
4701
PRFABSEL
PRINTER FIFO SELECTOR
APRFRD
APRFFF
APVIDEOR[7:0]
APVIDEDG[7:0]
APVIDEDB[7:0]
4702
PRINTER FIFO A 1024byte
BPRFRD
BPRFFF
BPVIDEOR[7:0]
BPVIDEDG[7:0]
BPVIDEDB[7:0]
PRINTER FIFO B 1024byte
4703
PRSDTREQ
PRSDTACK
PRNDTREQ
APRFWR
APRFEF
BPRFWR
BPRFEF
PFVIDEOR[7:0]
PFVIDEDG[7:0]
PFVIDEDB[7:0]
DATA SELECTOR
DATA TRANSFER CONTROL UNIT
PRMFWR
COPYMODE0
COPYMODE1
CONTROL REGISTER
IFWDATA[63:0]
DATA TRANSFER CONTROL UNIT
SVIDEOR[7:0]
SVIDEDG[7:0]
SVIDEDB[7:0]
SCANNER IMAGE PROCESS-ING UNIT

FIG. 47

FIG. 48


4302
4801
IFCLK
IFWDATA[63:0]
IFMAD [31:2]
ADDRESS SELECTOR
CHAIN CONTROLL -ER
MASTER DMA CONTROLL -ER
4802
4311
SCMD TREQ
SCANNER FIFIO CONTROLL -ER
IFMDTACK
IFMRW
IFMDTREQ
IFSDTREQ
IFSDTAC
IFSRW
MTSIZE[2:0]
IFSAD[6:0]
MASTER REQUEST ARBITER
SCMD TREQ
PRINTER FIFIO CONTROLL -ER
4312
4311
SCANNER FIFIO CONTROLL -ER
4312
SCANNER FIFIO CONTROLL -ER
L-BUS
TRANSFER ARBITER
4803
SCANNER VIDEO SYNCHRONIZING CONTROL UNIT
4306
PRINTER VIDEO SYNCHRONIZING CONTROL UNIT
4307
DATA SELECTOR
SCANNER VIDEO SYNCHRONIZING CONTROL UNIT
4306
PRINTER VIDEO SYNCHRONIZING CONTROL UNIT
4307
IFRDATA[63:0]
SCANNER FIFIO CONTROLLER
4311

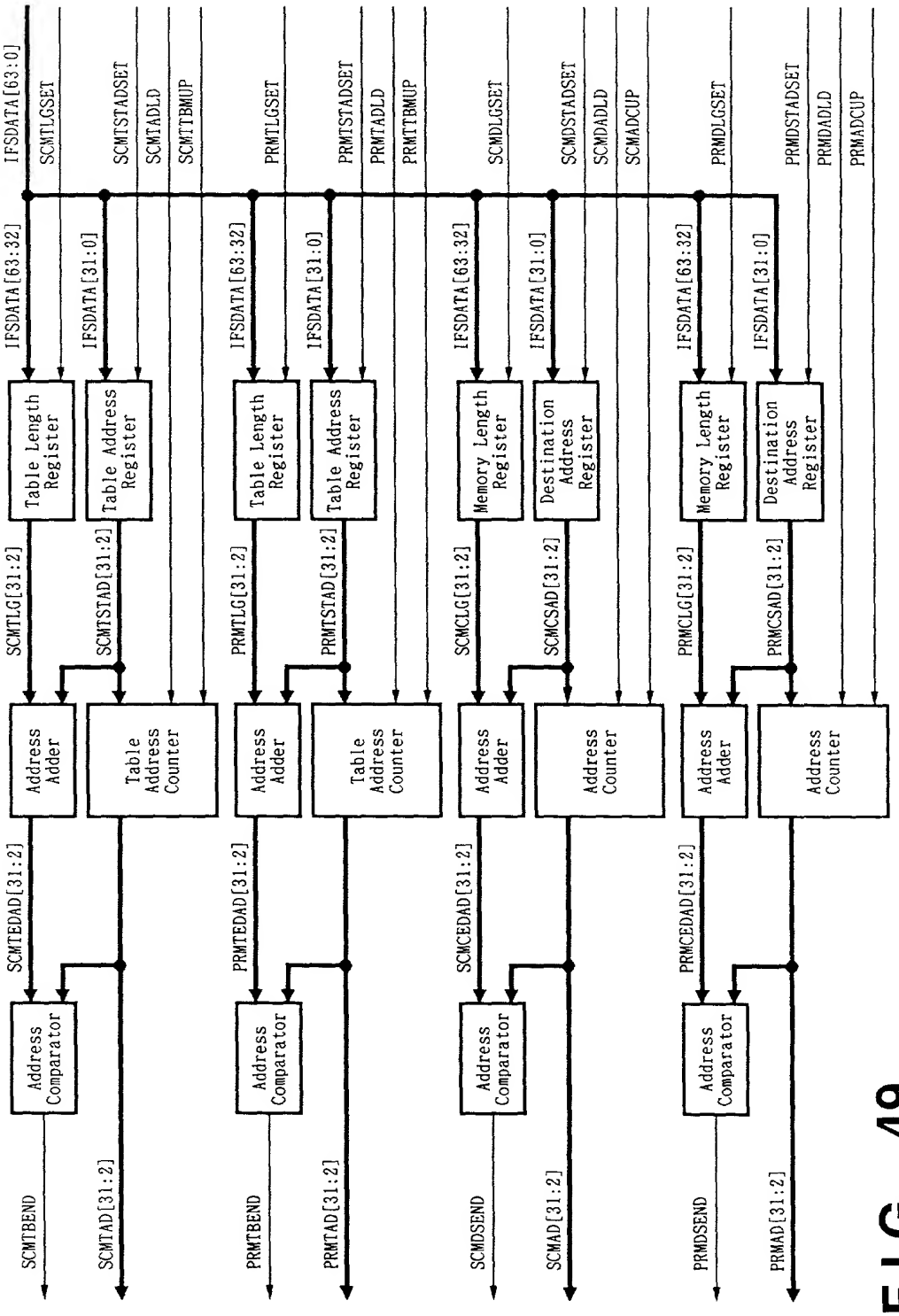

IFSDATA[63:0]
SCMTLGSET
SCMTSTADSET
SCMTADLD
SCMTTBMUP
PRMTLGSET
PRMTSTADSET
PRMTADLD
PRMTTBMUP
SCMDLGSET
SCMDSTADSET
SCMDADLD
SCMADCUP
PRMDLGSET
PRMDSTADSET
PRMDADLD
PRMADCUP
IFSDATA[63:32]
IFSDATA[31:0]
Table Length Register
Table Address Register
Memory Length Register
Destination Address Register
SCMTLG[31:2]
SCMTSTAD[31:2]
PRMTLG[31:2]
PRMTSTAD[31:2]
SCMCLG[31:2]
SCMCSAD[31:2]
PRMCLG[31:2]
PRMCSAD[31:2]
Address Adder
Table Address Counter
Address Counter
SCMTEDAD[31:2]
PRMTEDAD[31:2]
SCMCEDAD[31:2]
PRMCEDAD[31:2]
Address Comparator
SCMTBEND
SCMTAD[31:2]
PRMTBEND
PRMTAD[31:2]
SCMDSEND
SCMAD[31:2]
PRMDSEND
PRMAD[31:2]

FIG. 49

FIG. 50

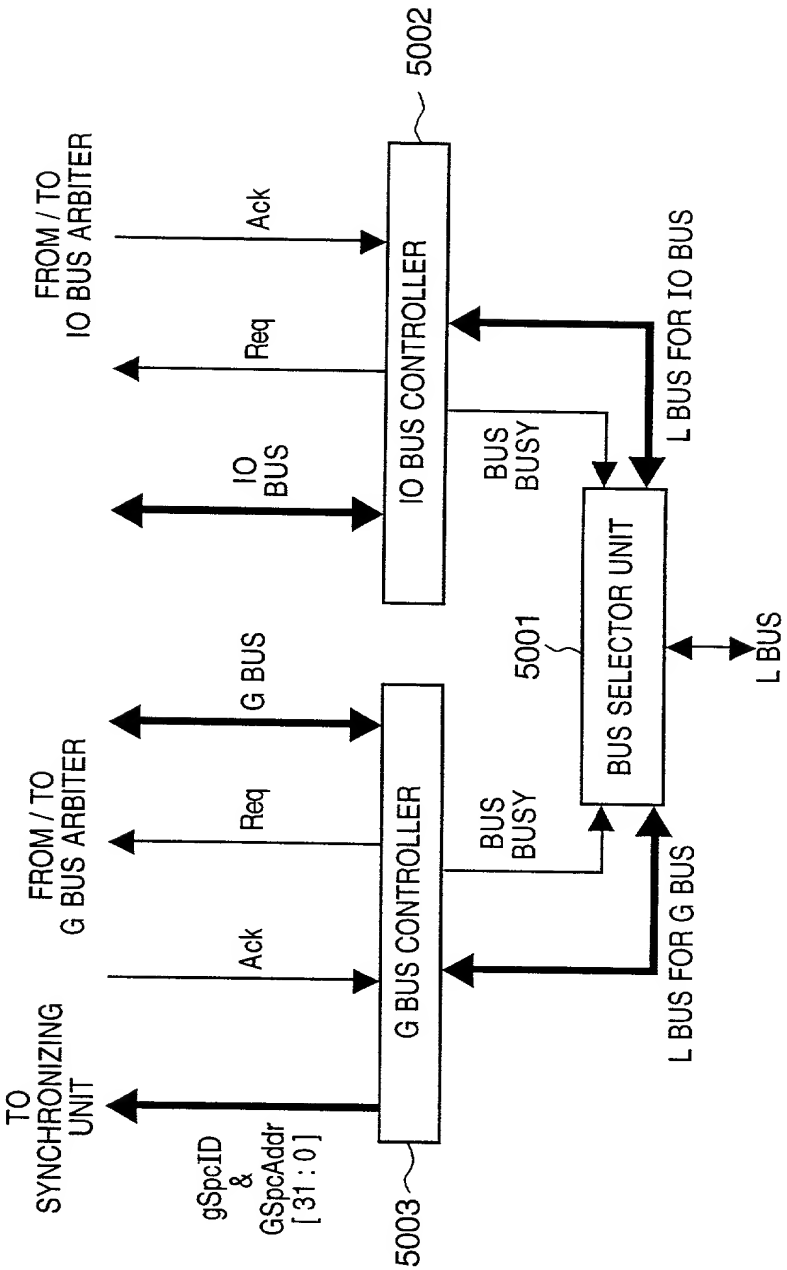
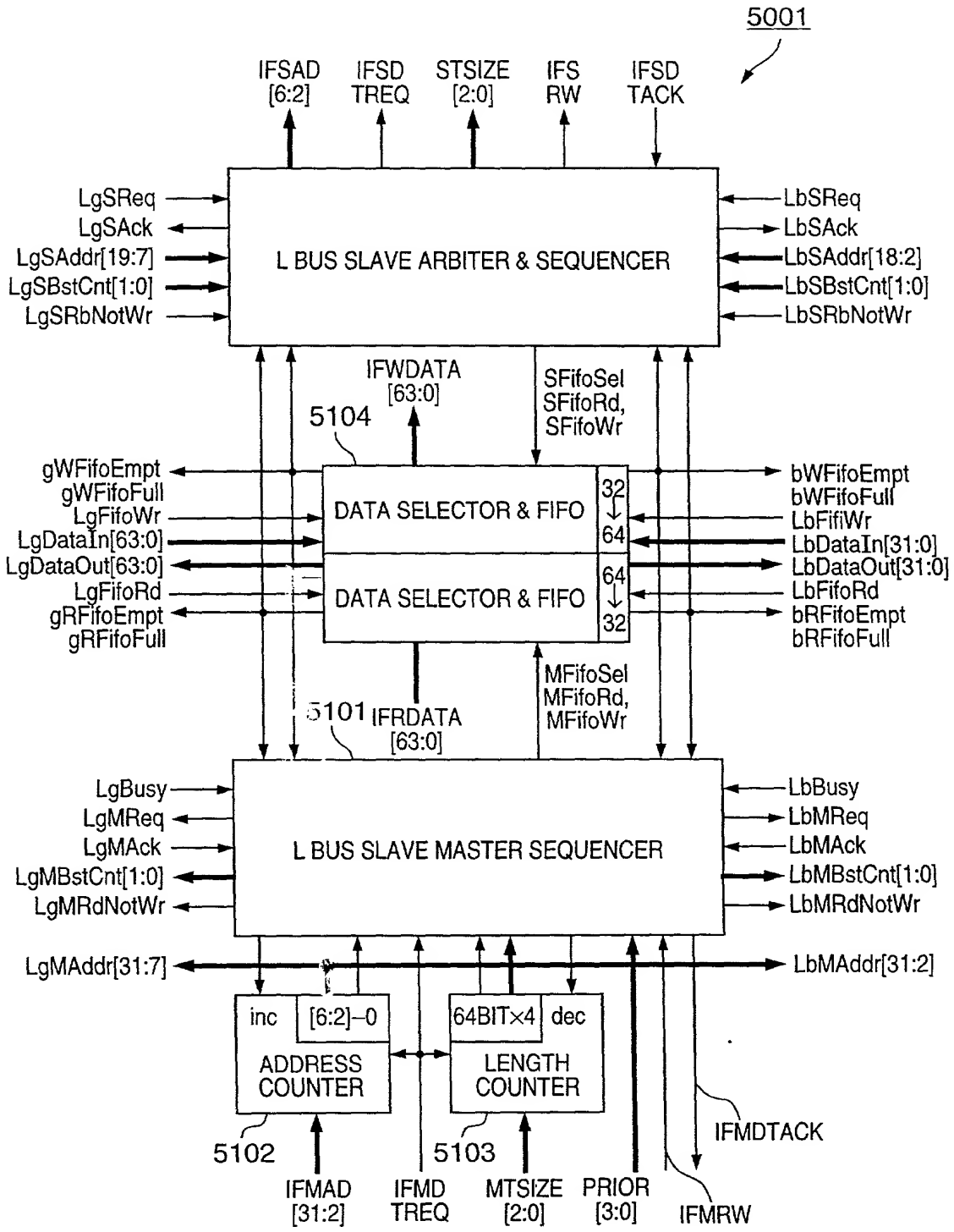

FROM / TO
IO BUS ARBITER
Ack
Req
IO
BUS
IO BUS CONTROLLER
5002
BUS
BUSY
L BUS FOR IO BUS
FROM / TO
G BUS ARBITER
Ack
Req
G BUS
G BUS CONTROLLER
BUS
BUSY
5001
BUS SELECTOR UNIT
L BUS
TO
SYNCHRONIZING
UNIT
gSpcID
&
GSpcAddr
[31:0]
5003
L BUS FOR G BUS

FIG. 51


5001
IFSAD [6:2]
IFSD TREQ
STSIZE [2:0]
IFS RW
IFSD TACK
LgSReq
LgSAck
LgSAddr[19:7]
LgSBstCnt[1:0]
LgSRbNotWr
L BUS SLAVE ARBITER & SEQUENCER
LbSReq
LbSAck
LbSAddr[18:2]
LbSBstCnt[1:0]
LbSRbNotWr
IFWDATA [63:0]
5104
SFifoSel SFifoRd, SFifoWr
gWFifoEmpt
gWFifoFull
LgFifoWr
LgDataIn[63:0]
LgDataOut[63:0]
LgFifoRd
gRFifoEmpt
gRFifoFull
DATA SELECTOR & FIFO
32
64
DATA SELECTOR & FIFO
64
32
bWFifoEmpt
bWFifoFull
LbFifiWr
LbDataIn[31:0]
LbDataOut[31:0]
LbFifoRd
bRFifoEmpt
bRFifoFull
MFifoSel MFifoRd, MFifoWr
5101
IFRDATA [63:0]
LgBusy
LgMReq
LgMAck
LgMBstCnt[1:0]
LgMRdNotWr
L BUS SLAVE MASTER SEQUENCER
LbBusy
LbMReq
LbMAck
LbMBstCnt[1:0]
LbMRdNotWr
LgMAddr[31:7]
LbMAddr[31:2]
inc
[6:2]–0
ADDRESS COUNTER
64BIT×4
dec
LENGTH COUNTER
IFMDTACK
5102
5103
IFMAD [31:2]
IFMD TREQ
MTSIZE [2:0]
PRIOR [3:0]
IFMRW

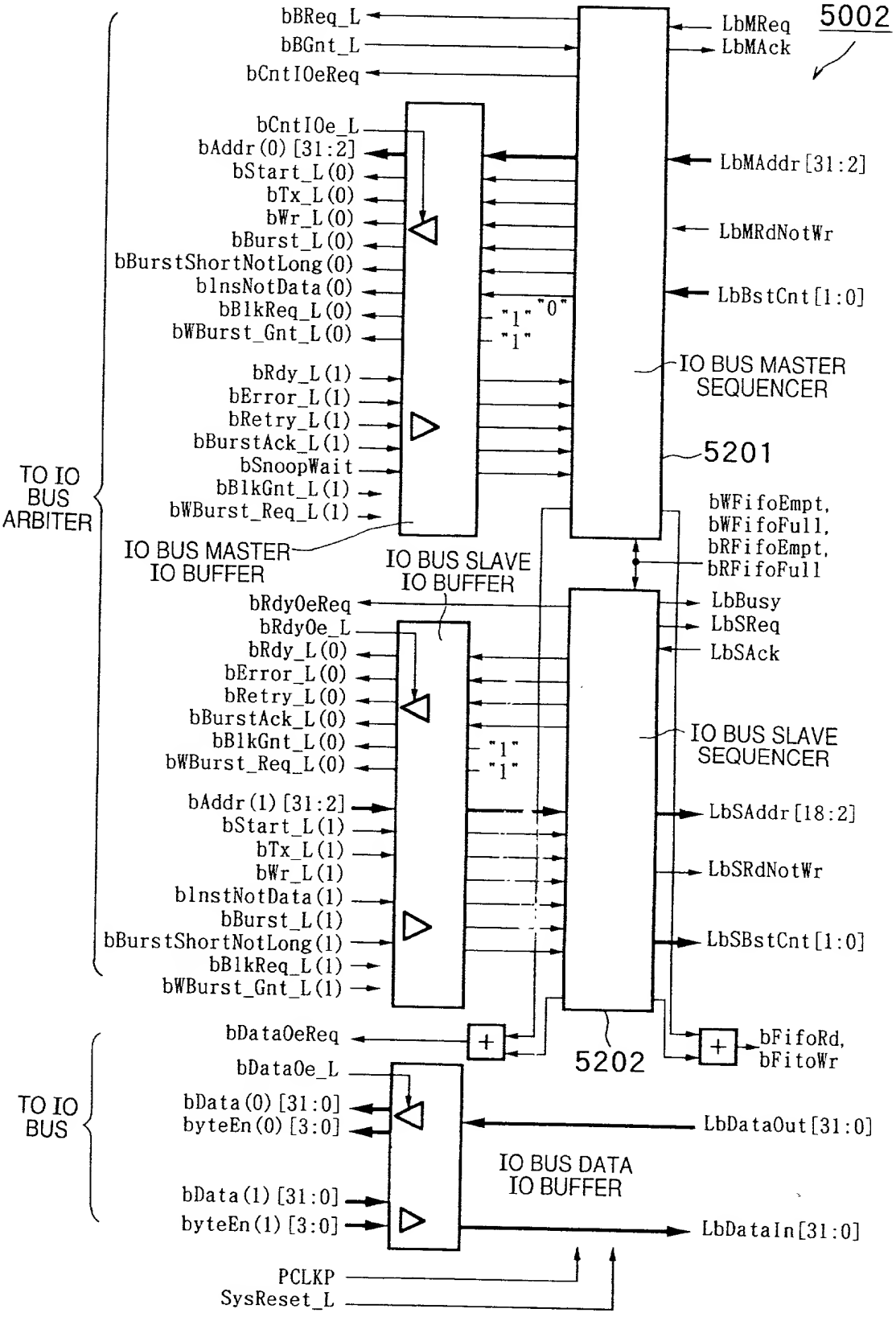

bBReq_L
bBGnt_L
bCntIOeReq
LbMReq
LbMAck
5002
bCntIOe_L
bAddr(0)[31:2]
bStart_L(0)
bTx_L(0)
bWr_L(0)
bBurst_L(0)
bBurstShortNotLong(0)
bInsNotData(0)
bBlkReq_L(0)
bWBurst_Gnt_L(0)
"1"
"0"
"1"
LbMAddr[31:2]
LbMRdNotWr
LbBstCnt[1:0]
IO BUS MASTER SEQUENCER
5201
bRdy_L(1)
bError_L(1)
bRetry_L(1)
bBurstAck_L(1)
bSnoopWait
bBlkGnt_L(1)
bWBurst_Req_L(1)
TO IO BUS ARBITER
IO BUS MASTER IO BUFFER
IO BUS SLAVE IO BUFFER
bWFifoEmpt,
bWFifoFull,
bRFifoEmpt,
bRFifoFull
bRdyOeReq
bRdyOe_L
bRdy_L(0)
bError_L(0)
bRetry_L(0)
bBurstAck_L(0)
bBlkGnt_L(0)
bWBurst_Req_L(0)
LbBusy
LbSReq
LbSAck
"1"
"1"
IO BUS SLAVE SEQUENCER
bAddr(1)[31:2]
bStart_L(1)
bTx_L(1)
bWr_L(1)
bInstNotData(1)
bBurst_L(1)
bBurstShortNotLong(1)
bBlkReq_L(1)
bWBurst_Gnt_L(1)
LbSAddr[18:2]
LbSRdNotWr
LbSBstCnt[1:0]
bDataOeReq
5202
bFifoRd,
bFitoWr
TO IO BUS
bDataOe_L
bData(0)[31:0]
byteEn(0)[3:0]
LbDataOut[31:0]
IO BUS DATA IO BUFFER
bData(1)[31:0]
byteEn(1)[3:0]
LbDataIn[31:0]
PCLKP
SysReset_L

FIG. 52

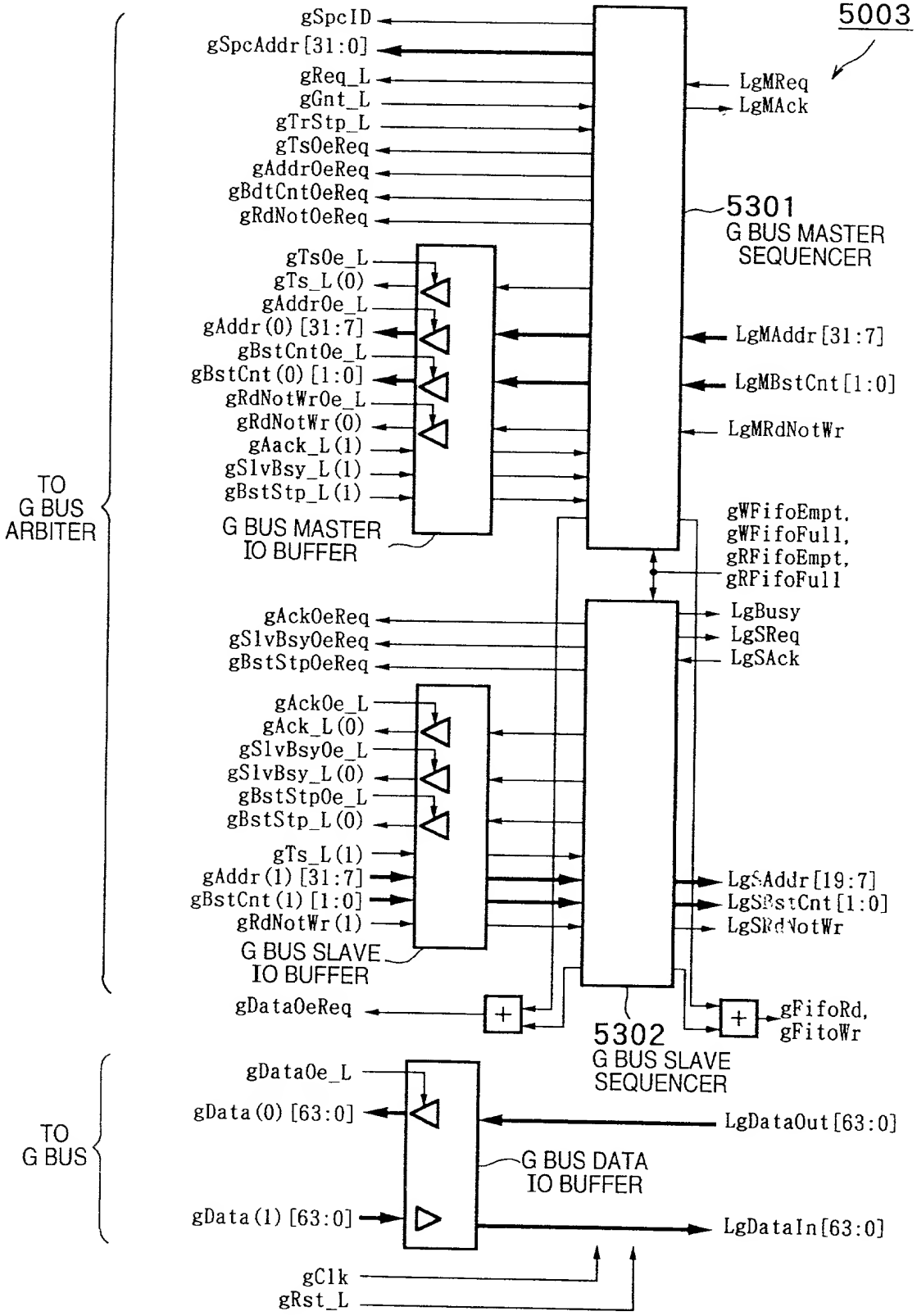

5003
gSpcID
gSpcAddr[31:0]
gReq_L
gGnt_L
gTrStp_L
gTsOeReq
gAddrOeReq
gBdtCntOeReq
gRdNotOeReq
LgMReq
LgMAck
5301
G BUS MASTER SEQUENCER
LgMAddr[31:7]
LgMBstCnt[1:0]
LgMRdNotWr
gTsOe_L
gTs_L(0)
gAddrOe_L
gAddr(0)[31:7]
gBstCntOe_L
gBstCnt(0)[1:0]
gRdNotWrOe_L
gRdNotWr(0)
gAack_L(1)
gSlvBsy_L(1)
gBstStp_L(1)
G BUS MASTER IO BUFFER
TO G BUS ARBITER
gWFifoEmpt,
gWFifoFull,
gRFifoEmpt,
gRFifoFull
gAckOeReq
gSlvBsyOeReq
gBstStpOeReq
LgBusy
LgSReq
LgSAck
gAckOe_L
gAck_L(0)
gSlvBsyOe_L
gSlvBsy_L(0)
gBstStpOe_L
gBstStp_L(0)
gTs_L(1)
gAddr(1)[31:7]
gBstCnt(1)[1:0]
gRdNotWr(1)
G BUS SLAVE IO BUFFER
LgSAddr[19:7]
LgSBstCnt[1:0]
LgSRdNotWr
gDataOeReq
gFifoRd,
gFitoWr
5302
G BUS SLAVE SEQUENCER
gDataOe_L
gData(0)[63:0]
LgDataOut[63:0]
G BUS DATA IO BUFFER
TO G BUS
gData(1)[63:0]
LgDataIn[63:0]
gClk
gRst_L

FIG. 53

FIG. 54

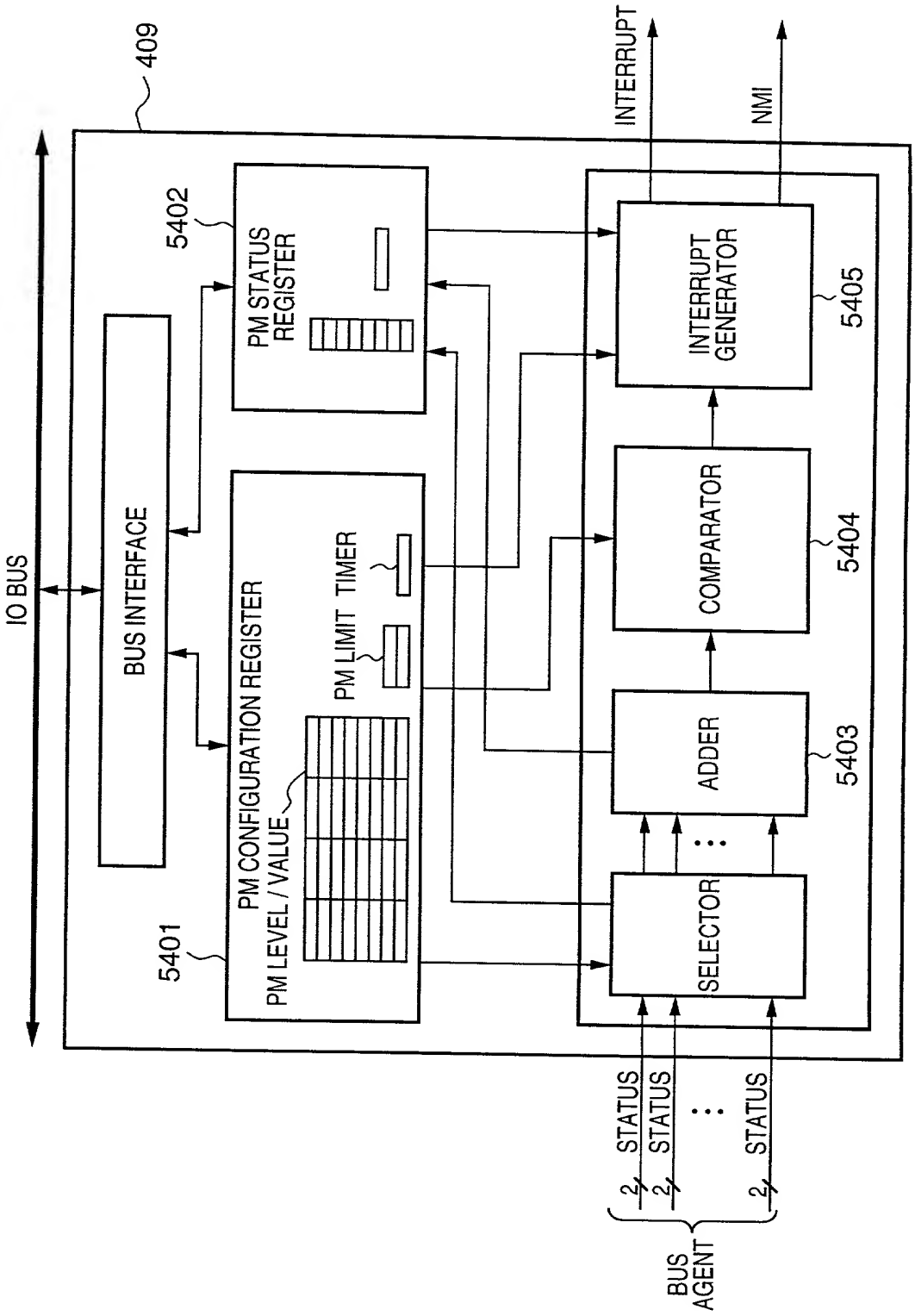
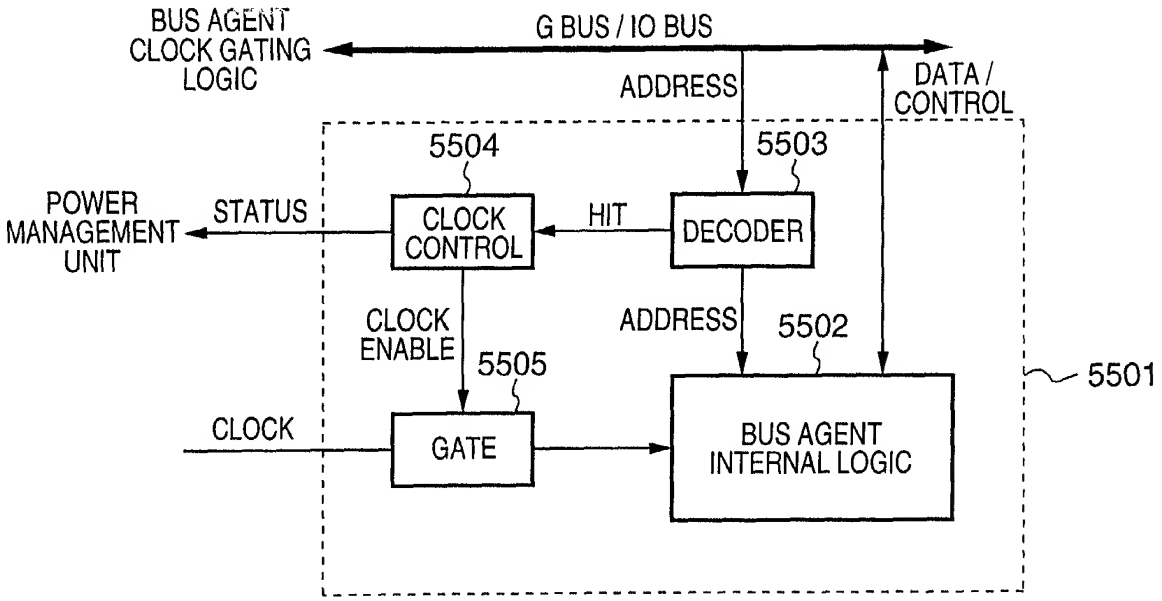

409
IO BUS
BUS INTERFACE
5401
PM CONFIGURATION REGISTER
PM LEVEL / VALUE
PM LIMIT TIMER
5402
PM STATUS REGISTER
SELECTOR
ADDER
5403
COMPARATOR
5404
INTERRUPT GENERATOR
5405
INTERRUPT
NMI
BUS AGENT
STATUS
STATUS
STATUS

FIG. 55



(CLOCK CONTROL)
- BUS AGENT DETECTS BUS ACTIVITY AND TURNS CLOCK ON AND OFF AUTOMATICALLY.
- THREE STATUS, NAMELY " SLEEP", " WAKE-UP" AND " WAIT".
- " SLEEP" IS A STATE IN WHICH BUS AGENT EXHIBITS NO ACTIVITY AND CLOCK HAS BEEN STOPPED.
- DECODER AND CLOCK CONTROLLER OPERATE EVEN IN SLEEP STATE;THEY MONITOR BUS AND WAIT FOR REQUEST.
- WHEN DECODER DETECTS ITS OWN ADDRESS, IT OPENS CLOCK GATE, ACTIVATES CLOCK OF INTERNAL LOGIC IS ACTIVATED AND COMPLIES WITH BUS REQUEST. STATE SHIFTS TO WAKE-UP.
- WHEN DATA TRANSFER ENDS,TRANSITION IS MADE TO WAIT STATE AND NEXT REQUEST IS AWAITED. CLOCK REMAINS ACTIVE. IF THERE IS REQUEST, WAKE-UP STATE IS RESTORED AND TRANSFER IS CARRIED OUT. COUNTING IS PERFORMED BY TIMER WHILE REQUEST IS BEING AWAITED. IF TIMER RUNS OUT OR TIME WITHOUT REQUEST BEING ISSUED, TRANSITION IS MADE TO SLEEP STATE AND CLOCK IS STOPPED.

FIG. 56

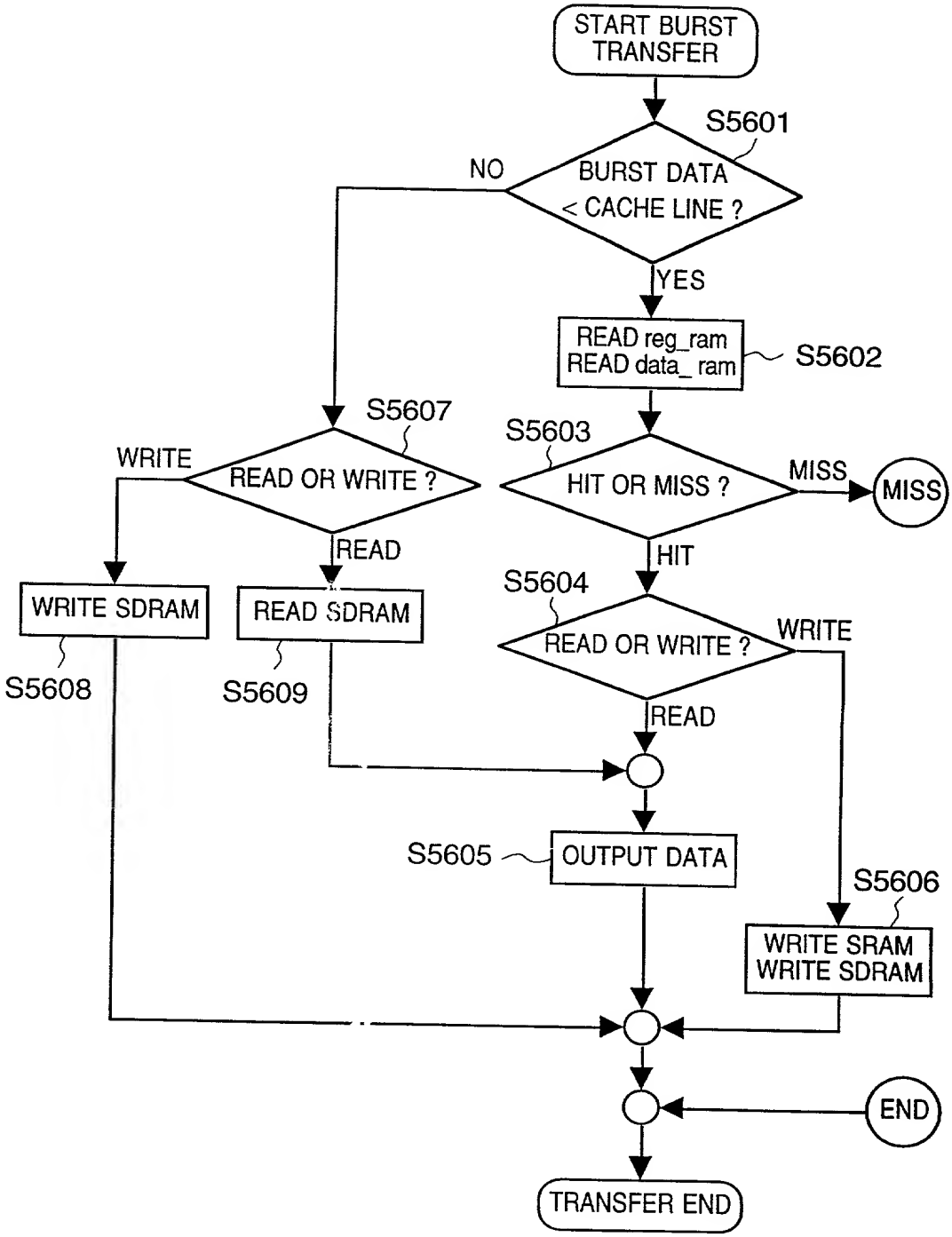

START BURST TRANSFER
S5601
BURST DATA < CACHE LINE ?
NO
YES
READ reg_ram READ data_ ram
S5602
S5603
HIT OR MISS ?
MISS
MISS
HIT
S5604
READ OR WRITE ?
WRITE
READ
S5607
READ OR WRITE ?
WRITE
READ
WRITE SDRAM
S5608
READ SDRAM
S5609
S5605
OUTPUT DATA
S5606
WRITE SRAM WRITE SDRAM
END
TRANSFER END

FIG. 57

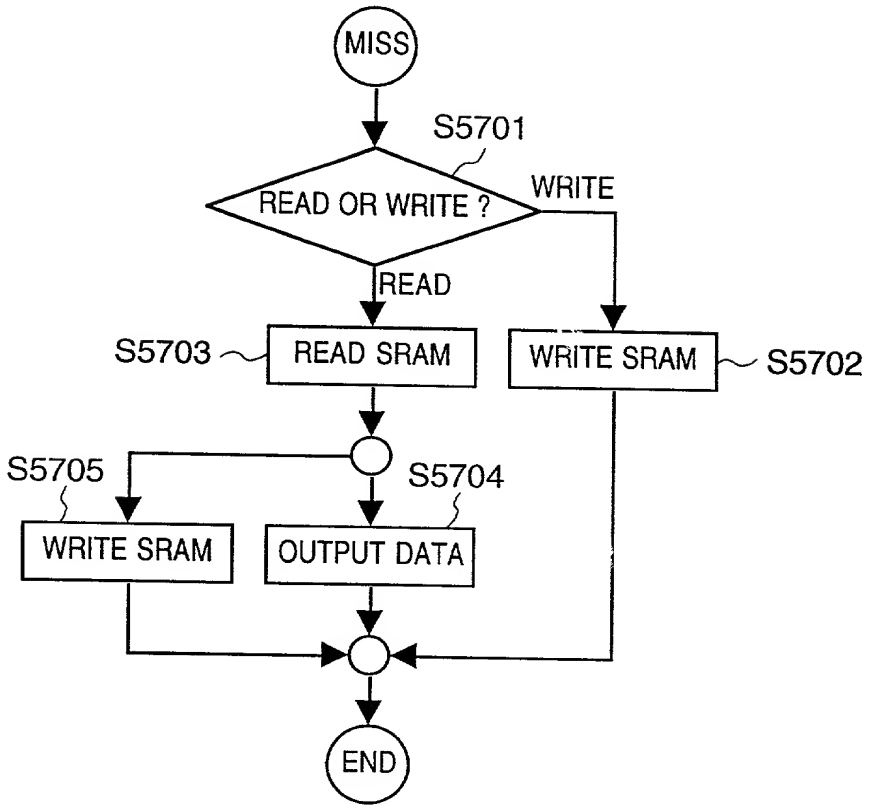

MISS
S5701
READ OR WRITE ?
WRITE
READ
S5703
READ SRAM
WRITE SRAM
S5702
S5705
S5704
WRITE SRAM
OUTPUT DATA
END

FIG. 58

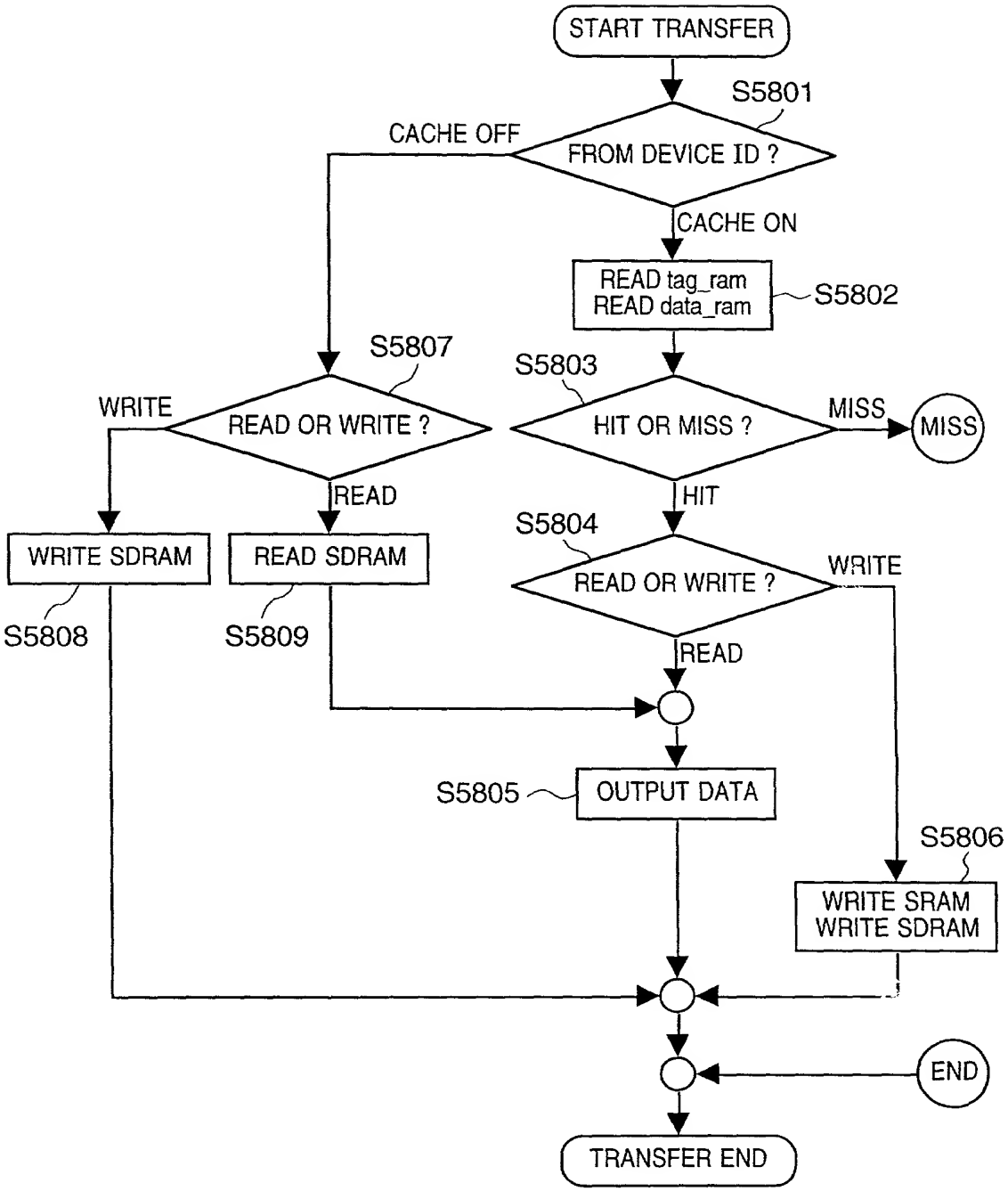
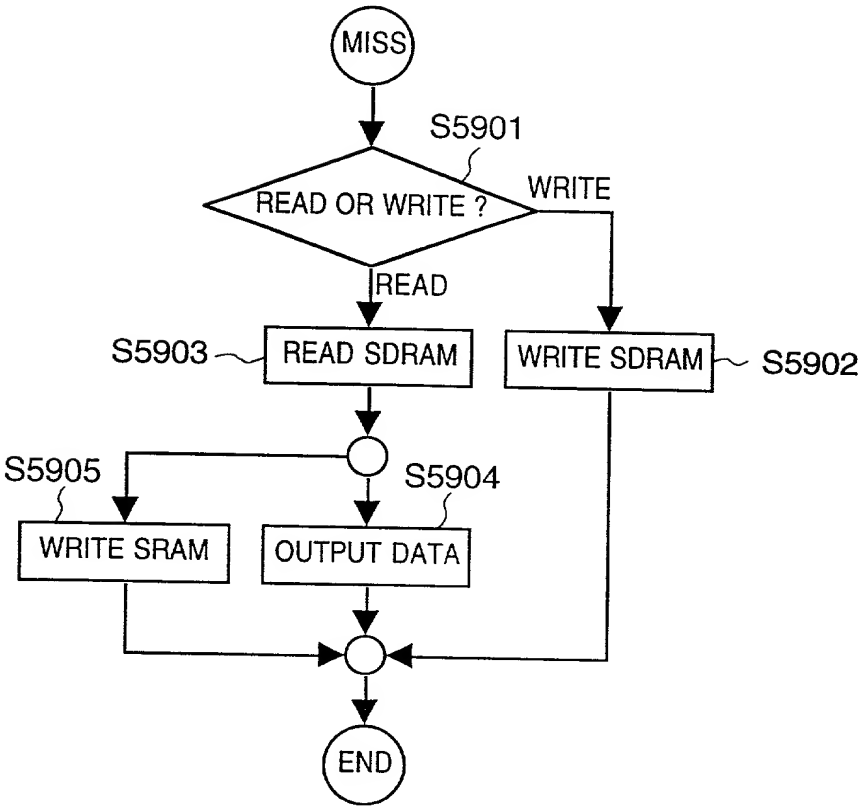

START TRANSFER
S5801
FROM DEVICE ID ?
CACHE OFF
CACHE ON
READ tag_ram
READ data_ram
S5802
S5807
S5803
WRITE
READ OR WRITE ?
HIT OR MISS ?
MISS
MISS
READ
HIT
S5804
WRITE SDRAM
READ SDRAM
READ OR WRITE ?
WRITE
S5808
S5809
READ
S5805
OUTPUT DATA
S5806
WRITE SRAM
WRITE SDRAM
END
TRANSFER END

FIG. 59


MISS
S5901
READ OR WRITE ?
WRITE
READ
S5903
READ SDRAM
WRITE SDRAM
S5902
S5905
S5904
WRITE SRAM
OUTPUT DATA
END